Radio Shack®

Service Manual

26-1080

TRS-80®

Model 4P, 4P Gate Array

Catalog Number 26-1080

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TRS-80® Model 4P/4P Gate Array Service Manual
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ADDENDA
A. Tandon Operating and Service Manual, *TM50-1 and TM50-2 5-1/4" Flexible Disk Drives*

MODEL 4P/4P GATE ARRAY HARDWARE

SECTION I

INTRODUCTION

INTRODUCTION

1.1 SYSTEM OVERVIEW

The TRS-80 Model 4P Microcomputer is a complete, self-contained portable (transportable) version of the popular TRS-80 Model 4 Microcomputer. It provides a carrying/protective case which has a recessed carrying handle, removable front cover which protects the CRT and disk drives and serves as a base when in the portable configuration, and self-contained keyboard conveniently stowed away in a recess in the main case. Power cord, floppy disk and manual storage are provided inside the removable cover/base. All connections to peripheral equipment are made at the rear of the Model 4P and optional feature connections are made by removing a rear cover plate. Proper care and handling must be observed to prevent damage to the computer.

The Model 4P is 100% compatible with all Model III and Model 4 disk software. System capability for Model III compatibility includes: Z80A CPU, 2 MHz operation, programmable RAM to emulate ROM for BASIC operating system, memory-mapped keyboard, memory-mapped video with 64-character by 16-line display, and full 48K Random Access Memory (RAM). Model 4 compatibility includes: Z80A CPU, 4 MHz operation, memory-mapped keyboard in upper memory, memory-mapped video in upper memory with 80-character by 24-line display, standard 64K RAM expandable to 128K RAM. Other standard features of the Model 4P which were options on the Model III and Model 4 are built-in FDC Circuit with two 184K Floppy Disk Drives and an RS-232-C Serial Communications Interface Circuit.

1.2 OPTIONAL FEATURES

Optional features available on the Model 4P include: 640 by 240 pixel High Resolution graphics Board, Direct-connect, auto-dial, auto-answer 300 bps Modem Board. The Model 4P does not support cassette operation or external Floppy Disk Drive.

TOP COVER/POWER SUPPLY
CASE
CRT
SWEEP
BOARD
REAR
MOUNTING
PLATE
CONTROL
MODULE
FAN
MAIN
CHASSIS
CRT
FRONT
BEZEL
PAN/MAIN
LOGIC PCB
DISK
DRIVE
ASSEMBLY
COVER/BASE
KEYBOARD

Figure 1-1.

1.3 SYSTEM BLOCK DIAGRAM

The System Block Diagram (Figure 1.2) shows the various internal components and connections of the Model 4P Microcomputer.

Figure 1-2. Model 4P Block Diagram

SECTION II

SPECIFICATIONS

SPECIFICATIONS

2.1 MICROPROCESSOR: 4 MHz Z80A, 8-bit CPU

Memory:	64K RAM bytes, expandable to 128K bytes 4K boot ROM, 2K video memory
Keyboard:	70-key standard typewriter keyboard, including 12-key numeric entry keypad. Special keys include BREAK, CTRL, CAPS, CLEAR, plus three programmable special function keys (F1, F2, and F3).
Video Display:	High-resolution 9" black and white display monitor with 64 or 32 characters per line by 16 lines in Model III mode and 80 or 40 characters per line by 24 lines in Model 4/4P mode. Displays upper and lower case ASCII characters, with descenders, 96 special characters, 64 alternate characters, 64 graphics characters, plus reverse video of all ASCII alpha-numeric characters.
Floppy Disk Drives:	Two built-in single-sided, double-density 5-1/4" thin-line floppy disk drives. Each drive stores up to 184K bytes. Data transfer rate is 250K bits per second.

2.2 PERIPHERAL INTERFACES

Standard:	I/O BUS for connection of hard disk and other peripherals.
	Serial Interface (RS-232-C port) One RS-232-C Serial Communications interface port which allows asynchronous and synchronous transmission. Mates with DB-25 connector on back of the Model 4P.
	Parallel Printer Interface Connection to a line printer via the 34-pin connector on the back of the Model 4P.
Optional:	640 x 240 High-Resolution graphics board
	Auto-answer Modem (300 baud)

2.3 POWER REQUIREMENTS

105-130 Vac, 60 Hz
240 Vac, 50 Hz (Australian)
220 Vac, 50 Hz (European)
Grounded Outlet

Maximum Current Drain: 1.7 Amperes

Typical Current Drain: 1.5 Amperes

2.4 OPERATING TEMPERATURE: 55 to 80° F (13 to 27° C)

2.5 DIMENSIONS: 9.3" H x 16.5" W x 13.25" D, 26 lbs carrying weight.

SECTION III

DISASSEMBLY/ASSEMBLY

DISASSEMBLY/ ASSEMBLY

3.1 OVERVIEW AND CASE

The Model 4P is modular in construction in that it can be disassembled in major component blocks after removal of the case cover. These major component blocks include the disk drives, the power supply, main CPU board, the CRT display, and the monitor board. Accessory components such as the power cord, additional diskettes, and operating manual can be stored in convenient recesses in the removable front cover/base. This cover/base provides protection for the CRT and disk drives during transport. It also serves as the base in the non-operating position of the computer.

The cover/base is held in place with snap locks on each side. These locks are positive action with a protective boss to prevent accidental opening of the cover/base. To remove, merely unsnap the lock and release the catch from the main assembly latch. The following procedures are noted in sequential order required to provide access to some of the components. Some parts removal does not require previous steps. Those which do are noted. For reassembly of unit, reverse order of disassembly instructions.

1. The main assembly of the Model 4P has a removable cover which allows access to all internal components when removed. Remove all connections to the rear of the unit. These include the AC power cord, printer cable, I/O port connector, and RS-232-C connector. The printer cable and I/O port connectors are edge card type connectors — exercise care in their removal.

2. Place the unit Bezel/CRT face-down on a soft surface to prevent damage to the CRT.

3. The case is held in place with six screws. Remove two screws from either side of the case at the front of the unit. To gain access to the last two screws, press down on one end of the carrying handle and then lift the handle from its recess. The final two case mounting screws are accessible under the handle assembly. These two screws attach the handle assembly as well as the case to the internal rear mounting plate.

4. After removing all six screws, lift the cover off the computer and set it aside for reassembly. Exercise care to prevent scratching or damaging the cover.

3.2 INTERNAL REAR MOUNTING PLATE

1. Remove the case from the unit as noted in Paragraph 3.1

2. The rear mounting plate serves to provide mounting for the case carrying handle and protection for the CRT. There are ten mounting screws which attach this plate to the main metal chassis of the computer. Four screws (Item 53 on exploded view p. 144, two on each side) mount the handle support (Item 16) and are accessible from the LH and RH side of the unit. With the rear of the unit toward you, two of these screws are located at the left just in front of the Disk Drive Assembly and accessible from the left side of the chassis assembly. The two on the right are accessible from the rear of the chassis assembly.

3. Six other screws are located around the outside edges of the rear mounting plate. Remove the plate and set it aside for reassembly.

3.3 FRONT BEZEL

1. The front bezel can be removed from the unit after the case and rear mounting plate have been removed as noted in Paragraphs 3.1 and 3.2.

2. Pull the brightness and contrast knobs off the pots from the front.

3. The rear mounting plate removal allows access to the six bezel-mounting screws. Four screws attach to the outside flanges of the metal chassis. The other two screws are located to the right of the metal partition separating the Disk Drives from the CRT section of the unit. Access to these two screws is with a long shank 1/4" nutdriver above and below the fan assembly.

4. Once these six screws are removed, remove the bezel and set it aside for reassembly. Exercise care in handling to prevent scratching or marring the surface.

3.4 TOP COVER/POWER SUPPLY

1. The Power Supply for the Model 4P is located on the underside of the top cover. Remove the case and rear terminal plate as noted in Paragraphs 3.1 and 3.2.

Figure 3-1. Bezel Mounting Screws

2. The cover is attached to the metal chassis with six screws. Remove these screws and then flip the cover to the right. A convenient arrangement for storing the cover/power supply while working on other modules is to reattach the cover/power supply to the chassis with two screws, allowing the assembly to rest above the disk drive assembly.

3. The power supply is attached to the top cover with four screws. Remove the connectors attached to the power supply at the left and then four screws to remove the supply completely from the unit.

4. When reassembling, ensure that the mylar insulator is positioned between the power supply and the top cover to provide proper insulation.

3.5 CATHODE RAY TUBE

The CRT is mechanically attached to the metal chassis with four screws which are accessible from the front of the unit.

1. Remove the case rear terminal cover, and top cover/power supply as noted in Paragraphs 3.1, 3.2, 3.3, and 3.4. This allows access to the connections on the CRT.

2. Disconnect the deflection yoke cable from the CRT PC board.

3. Disconnect the connector on the rear of the CRT neck which is attached to a small PC board.

WARNING

The anode of the CRT may have a high voltage charge. Before removing the high voltage (anode) lead, discharge the CRT as follows to prevent a serious shock. Connect one end of a wire to a known good ground and the other end of the wire to the metal shaft of an insulated-handle screwdriver. Insert the screwdriver blade under the suction cup and touch it to the clip holding the high voltage lead.

4. Disconnect the high voltage lead by inserting a grounded screwdriver under the cup. Use the screwdriver to compress the clip and pull the wire free.

5. Disconnect the ground wire (fastened at the splice) to the CRT neck connector PCB.

CAUTION:

If the CRT is dropped, it may implode. To avoid this kind of accident, carefully support the CRT when removing it from the chassis. Do not handle the CRT by the neck as this may cause the tube to break and cause personal injury.

6. Remove the four screws and washer from the front of the CRT which attach it to the metal chassis. Carefully slide the CRT out of the chassis through the front.

3.6 SWEEP BOARD

The CRT Sweep Board is accessible after the CRT is removed from the unit. It is mounted to the left side of the metal chassis with four screws. An insulated plate is located between the PCB and the metal chassis. Make sure this plate is in place on reassembly.

3.7 MAIN LOGIC PCB

The main logic PCB is a large board nested inside a metal pan at the bottom of the main metal chassis. To gain access to this assembly, remove unit parts as noted in Paragraphs 3.1 and 3.2. It is not necessary to remove the power supply assembly, or the CRT and associated PCB. Remove all connectors at the rear of the unit. These include the Modem connector, I/O port edge-card connector, printer edge-card connector, and floppy disk edge-card connector.

1. There are four screws on each side of the metal PCB mounting pan which attach the pan to the metal chassis. Remove these screws and the board and pan can be removed as a subassembly from the chassis.

2. At the front of the board, remove the four connectors at the left front of the board. These include the reset, video, and power connectors, and a grounding wire.

3. Nine screws attach the main logic PCB to the metal pan. The board is spaced away from the pan with raised bosses stamped into the pan.

3.8 KEYBOARD ASSEMBLY

1. The keyboard assembly is attached to the Main Logic PCB with a connector located at the right rear of the board. The PCB must be removed from the pan to allow this connector to be removed. Therefore, disassembly procedures for the main PCB must be followed.

2. The keyboard assembly is disassembled by removing the 7 mounting screws from the underside of the assembly. One of these screws is under a cork non-skid strip and care should be taken in removing this strip so that it is not ripped or punctured.

3. Remove the top cover, lift the keyboard PCB from its positioning bosses, and then remove the keyboard connector.

4. If the cable assembly requires replacement, feed the connector through the opening in the keyboard base, then install a tiewrap around the cable just before the insulation sleeve. This serves as a strain relief for the cable when the keyboard is reassembled. Ensure that this tiewrap is in the recess between the opening in the case and the clamping bosses on the bottom of the case.

5. Also ensure that on reassembly the PCB is properly positioned on the bosses of the base before attaching the top cover.

Figure 3-2. Keyboard Cable Strain Relief

3.9 DISK DRIVE ASSEMBLY

The disk drive assembly contains two floppy disk drives. It must be removed as a subassembly to the main metal chassis before the mounting screws for the drives themselves are accessible.

1. There are seven mounting screws which attach this subassembly to the main metal chassis, all of which are accessible from the right side of the unit. Four of these are located at the top of the assembly. Two screws are located under the disk drive assembly at the front, but accessible with a long shank screwdriver from the right side. A seventh screw mounts a tab to the metal chassis at the rear of the assembly.

2. After this subassembly is removed from the unit, screws which mount the drives in the housing are accessible. There are two screws at the top and one at the bottom.

NOTE:

Do not place a screw in the bottom rear mounting hole when reinstalling the disk drives into the metal housing. Installation of this screw can cause possible flexing of the drive and alignment problems.

Figure 3-3. Disk Drive Assembly

RH Side View

3.10 CONTROL MODULE

The control module is attached to the left front of the metal chassis with two screws. Remove component parts as noted in Paragraphs 3.1, 3.2, and 3.3 to allow access to the control module.

1. The module contains the unit power switch, reset switch, and brightness/contrast controls for the CRT display. All wiring to the control module is the plug-in kind attached to terminals or connectors from the rear of the module.

2. If the module is to be removed, tag all wiring so that proper reassembly is assured.

Figure 3-4. Control Module

SECTION IV

MAINTENANCE/TROUBLESHOOTING

MAINTENANCE/TROUBLESHOOTING

4.1 INTRODUCTION

This section is a general guide for use by service personnel. It contains the Maintenance and Troubleshooting procedures necessary to help isolate the problem area to a faulty board or subsystem. After board or subsystem has been identified, refer to specific section for more detailed troubleshooting information.

Refer to the schematics and the theory of operation during maintenance and troubleshooting for specific checkpoints and testing.

4.2 MAINTENANCE

The only part of the Model 4P that requires maintenance is the two Floppy Disk Drives. Periodical cleaning of the Read/Write Heads are recommended to assure error-free operation. For all other maintenance or alignments required, refer to Section 5.3 Mini-Disk Drives Maintenance Checks and Adjustments.

4.3 TROUBLESHOOTING

Please be sure that the power cord is properly connected to AC power before starting troubleshooting.

1. Turn Model 4P "ON" by toggling power switch. If power light indicator is on then go to **4**, if not, go to **2**.

2. Recheck AC power and power cord. If okay go to **3**, if bad replace or repair.

3. Check power switch and bulb. If okay go to **1**, if bad replace power switch or bulb.

4. Wait a few seconds for CRT to warm up. Adjust brightness and contrast at the front of console. If video display comes on go to **9**, if not go to **5**.

5. Check power switch. If okay go to **6**, if bad replace.

6. Check for AC power at input to power supply. If okay go to **7**, if bad replace or repair AC wiring harness.

7. Check power supply for correct output voltages. (Refer to Power Supply Section 5.4.) If okay go to **8**, if bad refer to Power Supply Troubleshooting 5.3.4.

8. Check for video and sync signals from Main Logic Board at J9. (Refer to CPU Board Section and Schematic.) If okay refer to CRT Display Adjustment Section 5.5.2, if bad refer to CPU Board Troubleshooting Section 5.1.17 or 5.2.17.

9. Does message "The Floppy Disk Drive Is Not Ready" appear? If yes go to **15**, if not go to **10**.

10. Does message "Close the Floppy Drive Door And Try Again" appear? If yes, go to **17**, if not go to **11**.

11. Does message "The Floppy Disk Drive Is Not Available" appear? If yes then go to **19**, if not go to **12**.

12. Does message "CRC Error, Try Again Or Use Another Disk" appear? If yes then go to **19**, if not go to **13**.

13. Does message "Seek Error, Try Again Or Use Another Disk" appear? If yes then go to **19**, if not go to **14**.

14. Does any other message appear? If yes then refer to Appendix B Startup Error Messages in Introduction to Your Disk System TRS-80 Model 4P, if not then go to **5**.

15. Insert Write Protected Diskette with TRSDOS 6.1.1 or later into Drive 0, close door and toggle RESET Switch. Does 4P boot up to TRSDOS Logo and prompt for date? If yes then go to **18**, if not then go to **16**.

16. Does message "The Floppy Disk Drive Is Not Ready" still appear? If yes then go to **17**, if not then go to **10**.

17. Try to boot again or use another diskette. If okay go to **18**. If still same message then go to **19**. If another message appears, go to **9**.

18. This indicates that the problem area exists on the Main Logic CPU Board. Refer to Section 5.1.17 or 5.2.17 CPU Board Troubleshooting for more detailed troubleshooting procedures.

19. This indicates a hardware failure of Floppy Disk interface or Floppy Disk Drive. Refer to Section 5.1.17 or 5.2.17 CPU Board Troubleshooting or Section 5.3 Mini-Disk Drive Maintenance Checks or Adjustments.

SECTION V

4P THEORY OF OPERATION

4P THEORY OF OPERATION

5.1 CPU THEORY OF OPERATION

5.1.1 Introduction

Contained in the following paragraphs is a description of the component parts of the Model 4P CPU. It is divided into the logical operational functions of the computer. All components are located on the Main CPU board inside the case housing. Refer to Section 3 for disassembly/assembly procedures.

5.1.2 Reset Circuit

The Model 4P reset circuit provides the neccessary reset pulses to all circuits during power up and reset operations. R25 and C218 provide a time constant which holds the input of U121 low during power-up. This allows power to be stable to all circuits before the RESET* and RESET signals are applied. When C218 charges to a logic high, the output of U121 triggers the input of a retriggerable one-shot multivibrator (U1). U1 outputs a pulse with an approximate width of 70 microsecs. When the reset switch is pressed on the front panel, this discharges C218 and holds the input of U121 low until the switch is released. On release of the switch, C218 again charges up, triggering U121 and U1 to reset the microcomputer.

5.1.3 CPU

The central processing unit (CPU) of the Model 4P microcomputer is a Z80A microprocessor. The Z80A is capable of running in either 2 MHz or 4 MHz mode. The CPU controls all functions of the microcomputer through use of its address lines (A0-A15), data lines (D0-D7), and control lines (/M1, /IOREQ, /RD, /WR, /MREQ, and /RFSH). The address lines (A0-A15) are buffered to other ICs through two 74LS244s (U68 and U26) which are enabled all the time with their enables pulled to GND. The control lines are buffered to other ICs through a 74F04 (U86). The data lines (D0-D7) are buffered through a bi-directional 74LS245 (U71) which is enabled by BUSEN* and the direction is controlled by BUSDIR*.

5.1.4 System Timing

The main timing reference of the microcomputer, with the exception of the FDC circuit, comes from a 20.2752 MHz Crystal Oscillator (Y1). This reference is divided and used for generating all necessary timing for the CPU, video circuit, and RS-232-C circuit. The output of the crystal oscillator is filtered by a ferritte bead (FB5), 470 ohm resistor (R46), and a 68 pf capacitor (C242). After being filtered, it is fed into U126, a 16R6A PAL (Programmable Array Logic), where it is divided by 2 to generate a 10.1376 MHz signal (10M) for the 64 X 16 video display. U126 divides the 20.2752 MHz by 4 to generate a 5.0688 MHz signal (RS232CLK) for the baud rate generator in the RS-232-C circuit. The CPU clock is also generated by U126 which can be either 2 or 4 MHz depending on the state of FAST input (pin 9 of U126). If FAST is a logic low, the 20.2752 MHz is divided by 10 which generates a 2.2752 MHz signal. If FAST is a logic high, the 20.2752 MHz is divided by 5 which generates a 4.05504 MHz signal. The CPU clock (PCLK) is fed through an active pull-up circuit which generates a full 5-volt swing with fast rise and fall times required by the Z80A. U126, the 16R6A PAL, generates all symmetrical output signals and also does not allow the PCLK output to short cycle or generate a low or high pulse under 110 nanoseconds which the Z80A also requires. Refer to System Timing Fig. 5-2.

5.1.4.1 Video Timing

The video timing is controlled by a 10L8 PAL (U127) and a four-bit synchronous counter U128 (74LS161). These two ICs generate all the necessary timing signals for the four video modes: 64 x 16, 32 x 16, 80 x 24, and 40 x 24. Two reference clock signals are required for the four video modes. One reference clock, the 10.1376 MHz signal (10M), is generated by U126 and is used by the 64 x 16 and 32 x 16 modes. The second reference clock is a 12.672 MHz (12M) signal which is generated by a Phase Locked Loop (PLL) circuit and is used by the 80 x 24 and 40 x 24 modes. The PLL circuit consists of U147 (74LS93), U148 (NE564 PLL), and U149 (74LS90). The original 20.2752 MHz clock is divided by 16 through U147 which generates a 1.2672 MHz signal. The output of U147 is reduced in amplitude by the voltage divider network R27 and R28 and the output is coupled to the reference input of U148 by C227.

The PLL (NE564) is adjusted to oscillate at 12.672 MHz by the tuning capacitor C231. This 12.672 MHz clock is then divided by 10 through U149 to generate a second 1.2672 MHz signal which is fed to a second input of U148. The two 1.2672 MHz signals are compared internally to the PLL where it corrects the 12.672 MHz output so it is synchronized with the 20.2752 MHz clock.

MODSEL and 8064* signals are used to select the desired video mode. 8064* controls which reference clock is used by U127 and MODSEL controls the single or double character width mode. Refer to the following chart for selecting each video mode.

8064*	MODSEL	Video Mode
0	0	64 x 16
0	1	32 x 16
1	0	80 x 24
1	1	40 x 24

*This is the state to be written to latch U89. Signal is inverted before being input to U127.

Figure 5-1. Model 4P Functional Block Diagram

Figure 5-2. System Timing

DCLK, the reference clock selected, is output from U127. DCLK is fed back into U127 for internal timing reference and is also fed to the clock input of U128 (74LS161). U128 is configured to preload with a count of 9 each time it reaches a count of 0. This generates a signal output of TC (128 pin 15) that occurs at the start of every character time of video output. TC is used to generate LOADS* (Load Shift Register). QA and QC of U128 are used to generate SHIFT*, XADR7*, CRTCLK and LOAD* for proper timing for the four video modes. QA, QB, and QC which are referred to as H, I, and J are fed to the Graphics Port J7 for reference timings of Hires graphics video. Refer to Video Timing, Figs. 5-3 and 5-4 for timing reference.

5.1.5 Address Decode

The Address Decode section will be divided into two subsections: Memory Map decoding and Port Map decoding.

5.1.5.1 Memory Map Decoding

Memory Map Decoding is accomplished by a 16L8 PAL (U109). Four memory map modes are available which are compatible with the Model III and Model 4 microcomputers. A second 16L8 PAL (U110) is used in conjunction with U109 for the memory map control which also controls page mapping of the 32K RAM pages. Refer to Memory Maps below.

5.1.5.2 Port Map Decoding

Port Map Decoding is accomplished by three 74LS138s (U87, U88, and U107). These ICs decode the low order address (A0-A7) from the CPU and decode the port being selected. The IN* signal from U108 enables U87 which allows the CPU to read from a selected port and the OUT* signal, also from U108, enables U88 which allows the CPU to write to the selected port. U107 only decodes the address and the IN* and OUT* signals are ANDed with the generated signals.

5.1.6 ROM

The Model 4P contains only a 4K x 8 Boot ROM (U70). This ROM is used only to boot up a Disk Operating System into the RAM memory. If Model III operation or DOS is required, then the RAM from location 0000-37FFH must be loaded with an image of the Model III or 4 ROM code and then executed. A system program called MODEL A/III is supplied with the Model 4P to provide the ROM image for proper Model III operation. On power-up, the Boot ROM is selected and mapped into location 0000-0FFFH. If the Boot ROM is not required after boot up, the Boot ROM must be mapped out by OUTing to port 9CH with D0 set or by selecting Memory Map modes 2 or 3. In Mode 1 the RAM is write enabled for the full 14K. This allows the RAM area mapped where Boot ROM is located to be written to while executing out of the Boot ROM. Refer to Memory Maps.

The Model 4P Boot ROM contains all the code necessary to initialize hardware, detect options selected from the keyboard, read a sector from a hard disk or floppy, and load a copy of the Model III ROM-Image (as mentioned) into the lower 14K of RAM.

The firmware is divided into the following routines:

* Hardware Initialization
* Keyboard Scanner
* Control
* Floppy and Hard Disk Driver
* Disk Directory Searcher
* File Loader
* Error Handler and Displayer
* RS-232 Boot
* Diagnostic Package

Theory of Operation

This section describes the operation of various routines in the ROM. Normally, the ROM is not addressable by normal use. However, there are several routines that are available through fixed calling locations and these may be used by operating systems that are booting.

On a power-up or RESET condition, the Z80's program counter is set to address 0 and the boot ROM is switched-in. The memory map of the system is set to Mode 0. (See Memory Map for details.) This will cause the Z80 to fetch instructions from the boot ROM.

The Initialization section of the Boot ROM now performs these functions:

1. Disables maskable and non-maskable interrupts
2. Interrupt mode 1 is selected
3. Programs the CRT Controller
4. Initializes the boot ROM control areas in RAM.
5. Sets up a stack pointer
6. Issues a Force Interrupt to the Floppy Disk Controller to abort any current activity
7. Sets the system clock to 4mhz
8. Sets the screen to 64 x 16
9. Disables reverse video and the alternate character sets
10. Tests for < . > key being pressed*
11. Clears all 2K of video memory

* This is a special test. If the < . > is being pressed, then control is transferred to the diagnostic package in the ROM. All other keys are scanned via the Keyboard Scanner.

Figure 5-3. Video Timing 64 x 16 Mode 80 x 24 Mode

Figure 5-4. Video Timing 32 x 16 Mode 40 x 24 Mode

The Keyboard scanner is now called. It scans the keyboard for a set period of time and returns several parameters based on which, if any, keys were pressed.

The keyboard scanner checks for several different groups of keys. These are shown below:

Function Group	Selection Group
<F1>	A
<F2>	B
<F3>	C
<1>	D
<2>	E
<3>	F
<Left-Shift>	G
<Right-Shift>	
<Ctrl>	
<Caps>	

Special Keys	Misc Keys
<P>	<Enter>
<L>	<Break>
<N>	

When any key in the Function Group is pressed, it is recorded in RAM and will be used by the Control routine in directing the action of the boot. If more than one of these keys are pressed during the keyboard scan, the last one detected will be the one that is used. The Function group keys are currently defined as:

<F1> or <1>	Will cause hard disk boot
<F2> or <2>	Will cause floppy disk boot
<F3> or <3>	Will force Model III mode
<Left-Shift>	Reserved for future use
<Right-Shift>	Boot from RS-232 port
<Ctrl>	Reserved for future use
<Caps>	Reserved for future use

The Special keys are commands to the Control routine which direct handling of the Model III ROM-image. Each key is detected individually.

<P>	When loading the Model III ROM-image, the user will be prompted when the disks can be switched or when ROM BASIC can be entered by pressing <Break>.
<N>	Instructs the Control routine to not load the Model III ROM-image, even if it appears that the operating system being booted requires it.
<L>	Instructs the Control routine to load the Model III ROM-image, even if it is already loaded. This is useful if the ROM-image has been corrupted or when switching ROM-images. (Note that this will not cause the ROM-image to be loaded if the boot sector check indicates that the Model III ROM image is not needed. Press <F3> or <F3> and <L> to accomplish that.

The Selection group keys are used in determining which file will be read from disk when the ROM-image is loaded. For details of this operation, see the Disk Directory Searcher. If more than one of the Selection group keys are pressed, the last one detected will be the one that is used.

The Miscellaneous keys are:

<Break>	Pressing this key is simply recorded by setting location 405BH non-zero. It is up to an operating system to use this flag if desired.
<Enter>	Terminates the Keyboard routine. Any other keys pressed up to that time will be acted upon. <Enter> is useful for experienced users who do not want to wait until the keyboard timer expires.

The Control section now takes over and follows the following flowchart.

Begin
<F1> or <1> pressed ?
Yes
1
Goto [1] (Hard Disk Boot)
No
<F2> or <2> pressed ?
Yes
2
Goto [2] (Floppy Disk Boot)
No
<F3> or <3> pressed ?
Yes
3
Goto [3] (Model III Boot)
No
<Right- Shift> pressed ?
Yes
4
Goto [4] (RS-232 Boot)
At this point, no valid Function keys have been pressed.
No
ARCNET Controller Board Present ?
Yes
Display an error message. (ARCNET Boot ROM required for ARCNET Boot)
No
1
A
A
Hard Disk Drive Present ?
Yes
Attempt to read boot sector
No
Yes
An error ?
<F1> or <1> pressed ?
Yes
Display Hard Disk Error Message
Stop
No
2
Floppy Disk Drive Present ?
Yes
Attempt to read boot sector
No
Yes
An error ?
No
B
C

B
C
<F2>
or <2>
pressed ?
Yes
Display
Floppy Disk
Error
Message
No
Stop
<N>
pressed
?
No
Sector
256 bytes,
and no ref.s
Model III
ROM ?
Note: 1
Yes
Yes
Set Transfer
Address to
43ØØH
Note: 2
F
Model III
ROM Image
Present ?
Note: 3
Yes
<L>
pressed
?
No
Yes
No
D
E

D
E
3
Set
Transfer
Address to
3Ø15H
Note: 2
F
Attempt to
locate
ROM Image
on
Floppy Disk
Note: 4
ROM
Image
Found ?
Note: 4
No
Yes
Write-enable
Ø-37FFH
(Mode 1)
Load ROM
Image
Note: 5
Errors
while loading
ROM Image ?
Yes
Display
Error
Message
Set Transfer
Address at end
of ROM Image
(Normally 3Ø15H)
Note: 2
Stop
G

G
ROM Image Present ?
No
Yes
<P> pressed ?
Yes
Display "ROM Image is loaded" message
Wait for <ENTER> or <BREAK> to be pressed
Write-protect memory (Mode Ø)
Set CPU speed to 2MHz
H

H
Switch boot ROM out of Memory
Jump to Transfer Address
7
Initialize RS-232 Port
Note: 6
Wait for Carrier Detect
Determine Correct Baud Rate
Transmit Baud Rate Detect Message
I

Notes:

(1) If the boot sector was not 256 bytes in length, then it is assumed to be a Model III package, and the ROM-image will be needed. If the sector is 256 bytes in length, then the sector is scanned for the sequence CDxx00H. The CD is the first byte of a Z80 unconditional subroutine call. The next byte can have any value. The third byte is tested against a zero. What this check does is test for any references to the first 256 bytes of memory. All Radio Shack Model III operating systems, and many other packages all reference the ROM at some point during the boot sector. Most boot sectors will display a message if the system cannot be loaded. To save space, these routines use the Model III ROM calls to display the message. Several ROM calls have their entry points in the first 256 bytes of memory, and these references are detected by the boot ROM. Packages that do not reference the Model III ROM in the boot sector can still cause the Model III ROM image to be loaded by coding a CDxx00 somewhere in the boot sector. It does not have to be executable. At the same time, Model 4 packages must take care that there is no sequence of bytes in the boot sector that could be mis-interpreted to be a reference to the Boot ROM. An example of this would be sequence 06CD0E00, which is a LD B,0CDH and a LD C,0. If the boot sector cannot be changed, then the user must press the <F3> key each time the system is started to inform the ROM that the disk contains a Model III package which needs the Model III ROM-image.

(2) If you are loading a Model 4 operating system, then the boot ROM will always transfer control to the first byte of the boot sector, which is at 4300H. If you are loading a Model III operating system or about to use Model III ROM BASIC, then the transfer address is 3015H. This is the address of a jump vector in the "C" ROM of the Model III ROM image, and this will cause the system to behave exactly like a Model III. If the ROM-image file that is loaded has a different transfer address, then that address will be used when loading is complete. If the image is already present, it will use 3015H.

(3) Two different tests are done to insure that the Model III ROM image is present. The first test is to check ever third location starting at 3000H for a C3H. This is done for 10 locations. If any of these locations does not contain a C3H, then the ROM image is considered to be "not present". The next test is to check two bytes at location 000BH. If these addresses contain E9E1H, then the ROM image is considered to be "present".

(4) See Disk Director Searcher for more information.

(5) See File Loader for more information.

(6) The RS-232 loader is described under RS-232 Boot.

Disk Directory Searcher

When the Model III ROM image is to be loaded, it is always read from the floppy in drive 0.

Before the operation begins, some checks are made. First, the boot sector is read in from the floppy and the first byte is checked to make sure it is either a 00H or a FEH. If the byte contains some other value, no attempt will be made to read the ROM image from that disk. The location of the directory cylinder is then taken from the boot sector and the type of disk is determined. This is done by examining the Data Address Mark that

was picked up by the Floppy Disk Controller (FDC) during the read of the sector. If the DAM equals 1, the disk is a TRSDOS 1.x style disk. If the DAM equals 0, then the disk is a LDOS 5.1/ TRSDOS 6 style disk. This is important since TRSDOS 1.x disks number sectors starting with 1 and LDOS style disks number sectors starting with 0.

Once the disk type has been determined, an extra test is made if the disk is a LDOS style disk. This test reads the Granule Allocation Table (GAT) to determine if the disk is single sided or double sided.

The directory is then read one record at a time and a compare is made against the pattern 'MODEL% ' for the filename and 'III' for the extension. The '%' means that any character will match this position. If the user pressed one of the selection keys (A-G) during the keyboard scan, then that character is substituted in place of the '%' character. For example, if you pressed 'D', then the search would be for the file 'MODELD ', with the extension 'III'. The searching algorithm searches until it finds the entry or it reaches the end of the directory.

Once the entry has been found, the extent information for that file is copied into a control block for later use.

File Loader

The file loader is actually two modules — the actual loader and a set of routines to fetch bytes from the file on disk. The loader is invoked via a RST 28H. The byte fetcher is called by the loader using RST 20H. Since restart vectors can be re-directed, the same loader is used by the RS-232 boot. The difference is that the RST 20H is redirected to point to the RS-232 data receiving routine. The loader reads standard loader records and acts upon two types:

01 Data Load
1 byte with length of block, including address
1 word with address to load the data
n bytes of data, where n + 2 equals the length specified

02 Transfer Address
1 byte with the value of 02
1 word with the address to start execution at.

Any other loader code is treated as a comment block and is ignored. Once an 02 record has been found, the loader stops reading, even if there is additional data, so be sure to place the 02 record at the end of the file.

Floppy and Hard Disk Driver

The disk drivers are entered via RST 8H and will read a sector anywhere on a floppy disk and anywhere on head 1 (top-head) in a hard disk drive. Either 256 or 512 byte sectors are readable by these routines and they make the determination of the sector size. The hard disk driver is compatible with both the WD1000 and the WD1010 controllers. The floppy disk driver is written for the WD1793 controller.

Serial Loader

Invoking the serial loader is similar to forcing a boot from hard disk or floppy. In this case the right shift key must be pressed at some time during the first three seconds after reset. The program does not care if the key is pressed forever, making it convenient to connect pins 8 and 10 of the keyboard connector with a shorting plug for bench testing of boards. This assumes that the object program being loaded does not care about the key closure.

Upon entry, the program first asserts DTR (J4 pin 20) and RTS (J4 pin 4) true. Next, "Not Ready" is printed on the topmost line of the video display. Modem status line CD (J4 pin 8) is then sampled. The program loops until it finds CD asserted true. At that time the message "Ready" is displayed. Then the program sets about determining the baud rate from the host computer.

To determine the baud rate, the program compares data received by the UART to a test byte equal to '55' hex. The receive is first set to 19200 baud. If ten bytes are received which are not equal to the test byte, the baud rate is reduced. This sequence is repeated until a valid test byte is received. If ten failures occur at 50 baud, the entire process begins again at 19200 baud. If a valid test byte is received, the program waits for ten more to arrive before concluding that it has determined the correct baud rate. If at this time an improper byte is received or a receiver error (overrun, framing, or parity) is intercepted, the task begins again at 19200 baud.

In order to get to this point, the host or the modem must assert CD true. The host must transmit a sequence of test bytes equal to '55' hex with 8 data bits, odd parity, and 1 or 2 stop bits. The test bytes should be separated by approximately 0.1 second to avoid overrun errors.

When the program has determined the baud rate, the message:

"Found Baud Rate x"

is displayed on the screen, where "x" is a letter from A to P, meaning:

A = 50 baud	E = 150	I = 1800	M = 4800
B = 75	F = 300	J = 2000	N = 7200
C = 110	G = 600	K = 2400	O = 9600
D = 134.5	H = 1200	L = 3600	P = 19200

The same message less the character signifying the baud rate is transmitted to the host, with the same baud rate and protocol. This message is the signal to the host to stop transmitting test bytes.

After the program has transmitted the baud rate message, it reads from the UART data register in order to clear any overrun error that may have occurred due to the test bytes coming in during the transmission of the message. This is because the receiver must be made ready to receive a sync byte signalling the beginning of the command file. For this reason, it is important that the host wait until the entire baud rate message (16 characters) is received before transmitting the sync byte, which is equal to 'FF' hex.

When the loader receives the sync byte, the message:

"Loading"

is displayed on the screen. Again, the same message is transmitted to the host, and, again, the host must wait for the entire transmission before starting into the command file.

If the receiver should intercept a receive error while waiting for the sync byte, the entire operation up to this point is aborted. The video display is cleared and the message:

"Error, x"

is displayed near the bottom of the screen, where "x" is a letter from B to H, meaning:

B = parity error
C = framing error
D = parity & framing errors
E = overrun error
F = parity & overrun errors
G = framing & overrun errors
H = parity & framing & overrun errors

The message:

"Error"

is then transmitted to the host. The entire process is then repeated from the "Not Ready" message. A six second delay is inserted before reinitialization. This is longer than the time required to transmit five bytes at 50 baud, so there is no need to be extra careful here.

If the sync byte is received without error, then the "Loading" message is transmitted and the program is ready to receive the command file. After receiving the "Loading" message the host can transmit the file without nulls or delays between bytes.

(Since the file represents Z80 machine code and all 256 combinations are meaningful, it would be disastrous to transmit nulls or other ASCII control codes as fillers, acknowledgement, or start-stop bytes. The only control codes needed are the standard command file control bytes.)

Data can be transmitted to the loader at 19200 baud with no delays inserted. Two stop bits are recommended at high baud rates.

See the File Loader description for more information on file loading.

If a receive error should occur during file loading, the abort procedure described above will take place, so when attempting remote control, it is wise to monitor the host receiver during transmission of the file. When the host is near the object board, as is the case in the factory application, or when more than one board is being loaded, it may be advantageous or even necessary to ignore the transmitted responses of the object board(s) and to manually pace the test byte, sync byte, and command file phases of the transmission process, using the video display for handshaking.

System Programmers Information

The Model 4P Boot ROM uses two areas of RAM while it is running. These are 4000H to 40FFH and 4300H to 43FFH. (For 512 byte boot sectors, the second area is 4300H to 44FFH.) If the Model III ROM Image is loaded, additional areas are used. See the technical reference manual for the system you are using for a list of these areas.

Operating systems that want to support a software restart by re-executing the contents of the boot ROM can accomplish this in one of two ways. If the operating system relies on the Model III ROM-Image, then jump to location 0 as you have in the past. If the operating system is a Model 4 mode package, a simple way is to code the following instructions in your assembly and load them before you want to reset:

Absolute Location	Instruction	
0000	DI	
0001	LD	A,1
0003	OUT	(9CH),A

These instructions cause the boot ROM to become addressable. After executing the OUT instruction, the next instruction executed will be one in the boot ROM. (These instructions also exist in the Model III ROM image at location 0.) The boot ROM has been written so that the first instruction is at address 0005. The hardware must be in memory mode 0 or else the boot ROM will not be switched in. This operation can be done with an OUT instruction and then a RST 0 can be executed to have the ROM switched in.

Restarts can be redirected at any time while the ROM is switched in. All restarts jump to fixed locations in RAM and these areas may be changed to point to the routine that is to be executed.

Restart	RAM Location	Default Use
0	none	Cold Start/Boot
8	4000H	Disk I/O Request
10	4003H	Display string
18	4006H	Display block
20	4009H	Byte Fetch (Called by Loader)
28	400CH	File Loader
30	400FH	Keyboard scanner
38	4012H	Reserved for future use
66	4015H	NMI (Floppy I/O Command Complete)

The above routines have fixed entry parameters. These are described here.

Disk I/O Request (RST 8H)

Accepts

A	1 for floppy, 2 for hard disk
B	Command Initialize 1 Restore 4 Seek 6 Read 12 (All reads have an implied seek)
C	Sector number to read The contents of the location disktype (405CH) are added to this value before an actual read. If the disk is a two sided floppy, just add 18 to the sector number.
DE	Cylinder number. (Only E is used in floppy operations)
HL	Address where data from a read operation is to be stored.

Returns

Z	Success, Operation Completed
NZ	Error, Error code in A

Error Codes

3	Hard Disk drive is not ready
4	Floppy disk drive is not ready
5	Hard Disk drive is not available
6	Floppy disk drive is not available
7	Drive Not Ready and no Index (Disk in drive, door open)
8	CRC Error
9	Seek Error
11	Lost Data
12	ID Not Found

Display String (RST 10H)

Accepts

HL	Pointer to text to be displayed. Text must be terminated with a null (0).
DE	Offset position on screen where text is to be displayed. (A 0000H will be the upper left-hand corner of the display.)

Returns

Success Always

A	Altered
DE	Points to next position on video
HL	Points to the null (0).

Display Block (RST 18H)

Accepts

HL Points to control vector in the format:

	+0	Screen Offset	
	+2	Pointer to text, terminated with null	
	+4	Pointer to text, terminated with null	
	..		
	+n	word FFFFH	End of control vector
or	+n	word FFFEH	Next word is new Screen Offset

If Z flag is set on entry, then the first screen offset is read from DE instead of from the control vector.

Each string is positioned after the previous string, unless a FFFEH entry is found. This is used heavily in the ROM to reduce duplication of words in error messages.

Returns

Success Always

DE	Points to next position on video

Byte Fetch (RST 20H)

Accepts None

Returns

Z	Success, byte in A
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call and:
2	ROM Image can't be loaded — Too many extents
10	ROM Image can't be loaded — Disk drive is not ready

File Loader (RST 28H)

Accepts None

Returns

Z	Success
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call of the byte fetch call and:
0	The ROM image was not found on drive 0

There are several pieces of information left in memory by the boot ROM which are useful to system programmers. These are shown below:

RAM Location	Description	
401DH	ROM Image Selected (% for none selected or A-G)	
4055H	Boot type	
	1 = Floppy	
	2 = Hard disk	
	3 = ARCNET	
	4 = RS-232C	
	5 - 7 = Reserved	
4056H	Boot Sector Size (1 for 256, 2 for 512)	
4057H	RS-232 Baud Rate (only valid on RS-232 boot)	
4059H	Function Key Selected	
	0 = No function key selected	
	<F1> or <1>	86
	<F2> or <2>	87
	<F3> or <3>	88
	<Caps>	85
	<Ctrl>	84
	<Left-Shift>	82
	<Right-Shift>	83
	Reserved	80-81 and 89-90
405BH	Break Key Indication (non-zero if <Break> pressed)	
405CH	Disk type	(0 for LDOS/ TRSDOS 6,1 for TRSDOS 1.x)

Keep in mind that Model III ROM image will initialize these areas, so this information is useful only to the Model 4 mode programmer.

5.1.7 RAM

Two configurations of Random Access Memory (RAM) are available on the Model 4P: 64K and 128K. The 64K and 128K option use the 6665-type 64K x 1 200NS Dynamic RAM, which requires only a single +5v supply voltage.

The DRAMs require multiplexed incoming address lines. This is accomplished by ICs U111 and U112 which are 74LS157 multiplexers. Data to and from the DRAMs are buffered by a 74LS245 (U117) which is controlled by Page Map PAL, U110. The proper timing signals RAS0*, RAS1*, MUX*, and CAS* are generated by a delay line circuit U97. U115 (1/2 of a 74S112) and U116 (1/4 of a 74F08) are used the generate a precharge circuit. During M1 cycles of the Z80A in 4 MHz mode, the high time in MREQ has a minimum time of 110 nanosecs. The specification of 6665 DRAM requires a minimum of 120 nanosecs so this circuit will shorten the MREQ signal during the M1 cycle. The resulting signal PMREQ is used to start a RAM memory cycle through U113 (a 74S64). Each different cycle is controlled at U113 to maintain a fast M1 cycle so no wait states are required. The output of U113 (PRAS*) is ANDed with RFSH to not allow MUX* and CAS* to be generated during a REFRESH cycle. PRAS* also generates either RAS0* or RAS1*, depending on which bank of RAM the CPU is selecting. GCAS* generated by the delay line U97 is latched by U115 (1/2 of a 74S112) and held to the end of the memory cycle. The output of U115 is ANDed with VIDEO signal to disable the CAS* signal from occurring if the cycle is a video memory access. Refer to M1 Cycle Timing (Figure 5-8. and 5-9.), Memory Read and Memory Write Cycle Timing (Figure 5-10.) and (Figure 5-11.).

	STATE	LEVEL
SELØ =	Ø	ØV
SEL1 =	Ø	ØV
ROM =	1	ØV

	STATE	LEVEL
SELØ =	Ø	ØV
SEL1 =	Ø	ØV
ROM =	Ø	5V

Figure 5-5. Memory

Figure 5-6. Memory

Figure 5-7. Memory

Figure 5-8. M1 Cycle Timing (2MHZ) 100ns/dir.

Figure 5-9. M1 Cycle Timing (4MHZ) 50ns/dir.

Figure 5-10. Memory Read Cycle Timing

Figure 5-11. Memory Write Cycle Timing

Memory Map — Model 4P

Mode 0

SEL0 = 0 = 0V
SEL1 = 0 = 0V
ROM = 1 = 0V

0000 — 0FFF	Boot ROM	4K
1000 — 37FF	RAM (Read Only)	10K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 0

SEL0 = 0 = 0V
SEL1 = 0 = 0V
ROM = 0 = +5V

0000 — 37FF	RAM (Read Only)	14K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1

SEL0 = 1 = +5V
SEL1 = 0 = 0V
ROM = 1 = 0V

0000 — 0FFF	Boot ROM	4K
0000 — 0FFF	RAM (Write Only)	4K
1000 — 37FF	RAM	10K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1

SEL0 = 1 = +5V
SEL1 = 0 = 0V
ROM = 0 = +5V

0000 — 37FF	RAM	14K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 2

SEL0 = 0 = 0V
SEL1 = 1 = +5V
ROM = X = Don't Care

0000 — F3FF	RAM	61K
F400 — F7FF	Keyboard	1K
F800 — FFFF	Video	2K

Mode 3

SEL0 = 1 = +5V
SEL1 = 1 = +5V
ROM = X = Don't Care

0000 — FFFF	RAM	64K

I/O Port Assignment

Port #	Normally Used	Out	In
FC — FF	FF	CASSOUT *	MODIN*
F8 — FB	F8	LPOUT *	LPIN*
F4 — F7	F4	DRVSEL *	(RESERVED)
F0 — F3	–	DISKOUT *	DISKIN *
F0	F0	FDC COMMAND REG.	FDC STATUS REG.
F1	F1	FDC TRACK REG.	FDC TRACK REG.
F2	F2	FDC SECTOR REG.	FDC SECTOR REG.
F3	F3	FDC DATA REG.	FDC DATA REG.
EC — EF	EC	MODOUT *	RTCIN *
E8 — EB	–	RS232OUT *	RS232IN *
E8	E8	UART MASTER RESET	MODEM STATUS
E9	E9	BAUD RATE GEN. REG.	(RESERVED)
EA	EA	UART CONTROL AND MODEM CONTROL REG.	UART STATUS REG.
EB	EB	UART TRANSMIT HOLDING REG.	UART HOLDING REG. (RESET D.R.)
E4 — E7	E4	WR NMI MASK REG. *	RD NMI STATUS *
E0 — E3	E0	WR INT MASK REG. *	RD INT MASK REG. *
A0 — DF	–	(RESERVED)	(RESERVED)
9C — 9F	9C	BOOT *	(RESERVED)
94 — 9B	–	(RESERVED)	(RESERVED)
90 — 93	90	SEN *	(RESERVED)
8C — 8F	–	GSEL0 *	GSEL0 *
88 — 8B	–	CRTCCS *	(RESERVED)
88, 8A	88	CRCT ADD. REG.	(RESERVED)
89, 8B	89	CRCT DATA REG.	(RESERVED)
84 — 87	84	OPREG *	(RESERVED)
80 — 83	–	GSEL1 *	GSEL1 *

I/O Port Description

Name: CASSOUT *
Port Address: FC — FF
Access: WRITE ONLY
Description: Output data to cassette or for sound generation

Note: The Model 4P **does not** support cassette storage, this port is only used to generate sound that was to be output via cassette port. The Model 4P sends data to onboard sound circuit.

D0 = Cassette output level (sound data output)

D1 = Reserved

D2 — D7 = Undefined

Name: MODIN * (CASSIN *)
Port Address: FC — FF
Access: READ ONLY
Description: Configuration Status

D0 = 0

D1 = CASSMOTORON STATUS

D2 = MODSEL STATUS

D3 = ENALTSET STATUS

D4 = ENEXTIO STATUS

D5 = (NOT USED)

D6 = FAST STATUS

D7 = 0

Name: LPOUT *
Port Address: F8 — FB
Access: WRITE ONLY
Description: Output data to line printer

D0 — D7 = ASCII BYTE TO BE PRINTED

Name: LPIN *
Port Address: F8 — FB
Access: READ ONLY
Description: Input line printer status

D0 — D3 = (RESERVED)

D4 = FAULT
1 = TRUE
0 = FALSE

D5 = UNIT SELECT
1 = TRUE
0 = FALSE

D6 = OUTPAPER
1 = TRUE
0 = FALSE

D7 = BUSY
1 = TRUE
0 = FALSE

Name: DRVSEL *
Port Address: F4 — F7
Access: WRITE ONLY
Description: Output FDC Configuration

Note: Output to this port will **ALWAYS** cause a 1-2 mscc. (Microsecond) wait to the Z80.

D0 = DRIVE SELECT 0

D1 = DRIVE SELECT 1

D2 = (RESERVED)

D3 = (RESERVED)

D4 = SDSEL
0 = SIDE 0
1 = SIDE 1

D5 = PRECOMPEN
0 = No write precompensation
1 = Write Precompensation enabled

D6 = WSGEN
0 = No wait state generated
1 = wait state generated

Note: This wait state is to sync Z80 with FDC chip during FDC operation.

D7 = DDEN *
0 = Single Density enabled (FM)
1 = Double Density enabled (MFM)

Name: DISKOUT *
Port Address: F0 — F3
Access: WRITE ONLY
Description: Output to FDC Control Registers

Port F0 = FDC Command Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignments)

Name: DISKIN *
Port Address: F0 — F3
Access: READ ONLY
Description: Input FDC Control Registers

Port F0 = FDC Status Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignment)

Name: MODOUT *
Port Address: EC — EF
Access: WRITE ONLY
Description: Output to Configuration Latch

D0 = (RESERVED)

D1 = CASSMOTORON (Sound enable)
0 = Cassette Motor Off (Sound enabled)
1 = Cassette Motor On (Sound disabled)

D2 = MODSEL
0 = 64 or 80 character mode
1 = 32 or 40 character mode

D3 = ENALTSET
0 = Alternate character set disabled
1 = Alternate character set enabled

D4 = ENEXTIO
0 = External IO Bus disabled
1 = External IO Bus enabled

D5 = (RESERVED)

D6 = FAST
0 = 2 MHZ Mode
1 = 4 MHZ Mode

D7 = (RESERVED)

Name: RTCIN *
Port Address: EC — EF
Access: READ ONLY
Description: Clear Real Time Clock Interrupt

D0 — D7 = DON'T CARE

Name: RS232OUT *
Port Address: E8 — EB
Access: WRITE ONLY
Description: UART Control, Data Control, Modem Control, BRG Control

Port E8 = UART Master Reset

Port E9 = BAUD Rate Gen. Register

Port EA = UART Control Register (Modem Control Reg.)

Port EB = UART Transmit Holding Reg.

(Refer to Model III or 4 Manual for Bit Assignments)

Name: RS232IN *
Port Address: E8 — EB
Access: READ ONLY
Description: Input UART and Modem Status

Port E8 = MODEM STATUS

Port E9 = (RESERVED)

Port EA = UART Status Register

Port EB = UART Receive Holding Register (Resets DR)

(Refer to Model III or 4 Manual for Bit Assignments)

Name: WRNMIMASKREG *
Port Address: E4 — E7
Access: WRITE ONLY
Description: Output NMI Latch

D0 — D5 = (RESERVED)

D6 = ENMOTOROFFINT
0 = Disables Motoroff NMI
1 = Enables Motoroff NMI

D7 = ENINTRQ
0 = Disables INTRQ NMI
1 = Enables INTRQ NMI

Name: RDNMISTATUS *
Port Address: E4 — E7
Access: READ ONLY
Description: Input NMI Status

D0 = 0

D2 — D4 = (RESERVED)

D5 = RESET (not needed)
0 = Reset Asserted (Problem)
1 = Reset Negated

D6 = MOTOROFF
0 = Motoroff Asserted
1 = Motoroff Negated

D7 = INTRQ
0 = INTRQ Asserted
1 = INTRQ Negated

Name: WRINTMASKREG *
Port Address: E0 — E3
Access: WRITE ONLY
Description: Output INT Latch

D0 — D1 = (RESERVED)

D2 = ENRTC
0 = Real time clock interrupt disabled
1 = Real time clock interrupt enabled

D3 = ENIOBUSINT
0 = External IO Bus interrupt disabled
1 = External IO Bus interrupt enabled

D4 = ENXMITINT
0 = RS232 Xmit Holding Reg. empty int. disabled
1 = RS232 Xmit Holding Reg. empty int. enabled

D5 = ENRECINT
0 = RS232 Rec. Data Reg. full int. disabled
1 = RS232 Rec. Data Reg. full int. enabled

D6 = ENERRORINT
0 = RS232 UART Error interrupts disabled
1 = RS232 UART Error interrupts enabled

D7 = (RESERVED)

Name: RDINTSTATUS *
Port Address: E0 — E3
Access: READ ONLY
Description: Input INT Status

D0 — D1 = (RESERVED)

D2 = RTC INT

D3 = IOBUS INT

D4 = RS232 XMIT INT

D5 = RS232 REC INT

D6 = RS232 UART ERROR INT

D7 = (RESERVED)

Name: BOOT *
Port Address: 9C — 9F
Access: WRITE ONLY
Description: Enable or Disable Boot ROM

D0 = ROM *
0 = Boot ROM Disabled
1 = Boot ROM Enabled

D1 — D7 = (RESERVED)

Name: SEN *
Port Address: 90 — 93
Access: WRITE ONLY
Description: Sound output

D0 = SOUND DATA

D1 — D7 = (RESERVED)

Name: OPREG *
Port Address: 84
Access: WRITE ONLY
Description: Output to operation reg.

D0 = SEL0

D1 = SEL1

SEL1	SEL0	MODE
0	0	0
0	1	1
1	0	2
1	1	3

D2 = 8064
0 = 64 character mode
1 = 80 character mode

D3 = INVERSE
0 = Inverse video disabled
1 = Inverse video enabled

D4 = SRCPAGE — Points to the page to be mapped as new page
0 = U64K, L32K Page
1 = U64K, U32K Page

D5 = ENPAGE — Enables mapping of new page
0 = Page mapping disabled
1 = Page mapping enabled

D6 = DESPAGE — Points to the page where new page is to be mapped
0 = L64K, U32K Page
1 = L64K, L32K Page

D7 = PAGE
0 = Page 0 of Video Memory
1 = Page 1 of Video Memory

5.1.8 Video Circuit

The heart of the video display circuit in the Model 4P is the 68045 Cathode Ray Tube Controller (CRTC), U85. The CRTC is a preprogrammed video controller that provides two screen formats: 64 by 16 and 80 by 24. The format is controlled by pin 3 of the CRTC (8064*). The CRTC generates all of the necessary signals required for the video display. These signals are VSYNC (Vertical Sync), HSYNC (Horizontal Sync) for proper sync of the monitor, DISPEN (Display Enable) which indicates when video data should be output to the monitor, the refresh memory addresses (MA0-MA13) which addresses the video RAM, and the row addresses (RA0-RA4) which indicates which scan line row is being displayed. The CRTC also provides hardware scrolling by writing to the internal Memory Start Address Register by OUTing to Port 88H. The internal cursor control of the 68045 is not used in the Model 4P video circuit.

Since the 80 by 24 screen requires 1,920 screen memory locations, a 2K by 8 static RAM (U82) is used for the video RAM. Addressing to the video RAM (U82) is provided by the 68045 when refreshing the screen and by the CPU when updating of the data is performed. These two sets of address lines are multiplexed by three 74LS157s (U83, U84, and U104). The multiplexers are switched by CRTCLK which allows the CRTC to address the video RAM during the high state of CRTCLK and the CPU access during the low state. A10 from the CPU is controlled by PAGE* which allows two display pages in the 64 by 16 format. When updates to the video RAM are performed by the CPU, the CPU is held in a WAIT state until the CRTC is not addressing the video RAM. This operation allows reads and writes to video RAM without causing hashing on the screen. The circuit that performs this function is a 74LS244 buffer (U103), an 8 bit transparent latch, 74LS373 (U102) and a Delay line circuit shared with Dynamic RAM timing circuit consisting of a 74LS74 (U95), 74LS32 (U94), 74LS04 (U74), 74LS00 (U96), 74LS02 (U75), and Delay Line (U97). During a CPU Read Access to the Video RAM, the address is decoded by the PAL U109 and asserts VIDEO* low. This is inverted by U74 (1/6 of 74LS04) which pulls one input of U96 (1/4 of 74LS00) and in turn asserts VWAIT * low to the CPU. RD is high at this time and is latched into U95 (1/2 of 74LS74) on the rising edge of XADR7*. XADR7* is inverse of CRTCLK which drives the CRTC (68045), and the address multiplexers U83, U84, and U104.

When RD is latched by U95, the Q output goes low releasing WAIT* from the CPU. The same signal also is sent to the Delay Line (U97) through U116 (1/4 of 74F08). The Delay line delays the falling edge 240 ns for VLATCH* which latches the read data from the video RAM at U102. The data is latched so the CRTC can refresh the next address location and prevent any hashing. MRD* decoded by U108 and a memory read is ORed with VIDEO* which enables the data from U102 to the data bus. The CPU then reads the data and completes the cycle. A CPU write is slightly more complex in operation. As in the RD cycle, VIDEO* is asserted low which asserts VWAIT* low to the CPU. WR is high at this time which is NANDed with VIDEO and synced with CRTCLK to create VRAMDIS that disables the video RAM output. On the rising edge of XADR7*, WR is latched into U95 (1/2 of 74LS74) which releases VWAIT* and starts cycle through the Delay Line. After 30ns DLYVWR* (Delayed video write) is asserted low which also asserts VBUFEN* (Video Buffer Enable) low. VBUFEN* enabled data from the Data bus to the video RAM. Approximately 120ns later DLYVWR* is negated high which writes the data to the video RAM and negates VBUFEN* turning off buffer. The CPU then completes WR cycle to the video RAM. Refer to Video RAM CPU Access Timing Figure 5-12 for timing of above RD or WR cycles.

During screen refresh, CRTCLK is high allowing the CRTC to address Video RAM. The data out of the video RAM is latched by LOAD* into a 74LS273 (U101). D7 is generated by INVERSE* through U125 (1/6 of 74S04), and U123 (1/4 of 74LS08). This decoding determines if character should be alpha-numeric only (if inverse high) or unchanged (INVERSE* low). The outputs of U101 are used as address inputs the character generator ROM (U42). A9 is decoded with ENALTSET (Enable Alternate Set) and Q7 of U101, which resets A9 to a low if Q7 and ENALTSET are high. See ENALTSET Control Table below.

ENALTSET	Q7	Q6	A9
0	0	0	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

FIGURE 5-12. Video RAM CPU Access Timing

RA0-RA3, row addresses from the CRTC are used to control which scan line is being displayed. The Model 4P has a 4-bit full adder 74LS283 (U61) to modify the Row address. During a character display DLYGRAPHIC* is high which applies a high to all 4 bits to be added to row address. This will result in subtracting one from Row address count and allow all characters to be displayed one scan line lower. The purpose is so inverse characters will appear within the inverse block. When a graphic block is displayed DLYGRAPHIC* is low which causes the row address to be unmodified. Moving jumper from E14-E15 to E15-E16 will disable this circuit.

DLYCHAR* and DLYGRAPHICS are inverse signals and control which data is to be loaded into the shift register U63. When DLYCHAR* is low and DLYGRAPHIC* is high, the Character Generator ROM (U42) is enabled to output data: when DLYCHAR* is high and DLYGRAPHIC* is low the graphics characters from U41 (74LS15) is buffered by U43 (74LS244) to the shift register. The data is loaded into the shift register on the rising edge of SHIFT* when LOADS* is low. Blanking is accomplished by masking off LOADS* so no data will be loaded and zero data will be shifted out with the serial input of U63, pin 1, grounded. Serial video data is output U63 pin 13 and is mixed with inverse and/or hires graphics information by (1/4 or 74LS86) U143. The video data is then mixed with a DO7 Rate clock, either DOT* and DCLK, to create distinct dots on the monitor. DOT* and DCLK are inverse signals and are provided to allow a choice to obtain the best video results. The video information is filtered by F34, R45 (47 ohm resistor), and C241 (100 pf Cap) and output to video monitor. VSYNC and HSYNC are buffered by (1/2 of 74LS86) U143 and are also output to video monitor. Refer to Video Circuit Timing Figure 5-13, Video Blanking Timing Figure 5-14., and Inverse Video Timing Figure 5-1 for timing relationships of Video Circuit.

5.1.9 Keyboard

The keyboard interface of the Model 4P consists of open collector drivers which drive an 8 by 8 key matrix keyboard and an inverting buffer which buffers the key or keys pressed on the data bus. The open collector drivers (U56 and U57 (7416) are driven by address lines A0-A7 which drive the column lines of the keyboard matrix. The ROW lines of the keyboard are pulled up by a 1.5 kohm resistor pack RP2. The ROW lines are buffered and inverted onto the data bus by U58 (74LS240) which is enabled when KEYBD* is a logic low. KEYBD* is a memory mapped decode of addresses 3800-3BFF in Model III Mode and F400-F7FF in Model 4/4P mode. Refer to the Memory Map under Address Decode for more information. During real time operation, the CPU will scan the keyboard periodically to check if any keys are pressed. If no key is pressed, the resistor pack RP2 keeps the inputs of U58 at a logic high. U58 inverts the data to a logic low and buffers it to the data bus which is read by the CPU. If a key is pressed when the CPU scans the correct column line, the key pressed will pull the corresponding row to a logic low. U58 inverts the signal to a logic high which is read by the CPU.

5.1.10 Real Time Clock

The Real Time Clock circuit in the Model 4P provides a 30 Hz (in the 2 MHz CPU mode) or 60 Hz (in the 4 MHz CPU mode) interrupt to the CPU. By counting the number of interrupts that have occurred, the CPU can keep track of the time. The 60 Hz vertical sync signal (VSYNC) from the video circuitry is used for the Real Time Clock's reference. In the 2 MHz mode, FAST is a logic low which sets the Preset input, pin 4 of U22 (74LS74), to a logic high. This allows the 60 Hz (VSYNC) to be divided by 2 to 30 Hz. The output of 1/2 of U22 is ORed with the original 60 Hz and then clocks another 74LS74 (1/2 of U22). If the real time clock is enabled (ENRTC at a logic high), the interrupt is latched and pulls the INT* line low to the CPU. When the CPU recognizes the interrupt, the pulse is counted and the latch reset by pulling RTCIN* low. In the 4 MHz mode, FAST is a logic high which keeps the first half of U22 in a preset state (the Q* output at a logic low). The 60 Hz is used to clock the interrupts.

NOTE: If interrupts are disabled, the accuracy of the real time clock will suffer.

5.1.11 Line Printer Port

The Line Printer Port Interface consists of a pulse generator, an eight-bit latch, and a status line buffer. The status of the line printer is read by the CPU by enabling buffer U3 (74LS244). This buffer is enabled by LPRD* which is a memory map and port map decode. In Model III mode, only the status can be read from memory location 37E8 or 37E9. The status can be read in all modes by an input from ports F8-FB. For a listing of the bit status, refer to Port Map section.

After the printer driver software determines that the printer is ready for printing (by reading the correct status), the characters to be printed are output to Port F8-FB. U2, a 74LS374 eight-bit latch, latches the character byte and outputs to the line printer. One-half of U1 (74LS123), a one-shot, is then triggered which generates an appropriate strobe signal to the printer which signifies a valid character is ready. The output of the one-shot is buffered by 1/6th of the U21 (74LS04) to prevent noise from the printer cable from flase-triggering the one-shot.

Figure 5-13. Video Circuit Timing

Figure 5-14. Video Blanking Timing

Figure 5-15. Inverse Video Timing

5.1.12 Graphics Port

The Graphics Port (J7) on the Model 4P is provided to attach the optional Graphics Board. The port provides D0-D7 (Data Lines), A0-A3 (Address Lines), IN*, GEN* and RESET* for the necessary interface signals for the Graphics Board. GEN* is generated by negative ORing Port selects GSEL0* (8C-8FH) and GSELI* (80-83H) together by (1/4 of 74LS08) U23. The resulting signal is negative ANDed with IORQ* by (1/4 of 74S32) U62. Seven timing signals are provided to allow synchronization of Main Logic Board Video and Graphics Board Video. These timing signals are VSYNC, HSYNC, DISPEN, DCLK, H, I, and J. Three control signals from the Graphics Board are used to sync to CPU access and select different video modes. WAIT* controls the CPU access by causing the CPU to WAIT till video is in retrace area before allowing any writes or reads to Graphics Board RAM. ENGRAF is asserted when Graphics video is displayed. ENGRAF also disables inverse video mode on Main Logic Board Video. CL166* (Clear 74L166) is used to enable or disable mixing of Main Logic Board Video and Graphics Board Video. If CL166* is negated high, then mixing is allowed in all for video modes 80 x 24, 40 x 24, 64 x 16, and 32 x 16. If CL166* is asserted low, this will clear the video shift register U63, which allows no video from the Main Logic Board. In this state 8064* is automatically asserted low to put screen in 80 x 24 video mode. Refer to Figure 5-16. Graphic Board Video Timing for timing relationships. Refer to the Model 4/4P Graphics Board Service information for service or technical information on the Graphics Board.

5.1.13 Sound

The sound circuit in the Model 4P is compatible with the Sound Board which was optional in the Model 4. Sound is generated by alternately setting and clearing data bit D0 during an OUT to port 90H. The state of D0 is latched by U130 (1/2 of a 74LS74) and the output is amplified by Q2 which drives a piezoelectric sound transducer. The speed of the software loop determines the frequency, and thus, the pitch of the resulting tone. Since the Model 4P does not have a cassette circuit, some existing software that used the cassette output for sound would have been lost. The Model 4P routes the cassette latch to the sound board through U142. When the CASSMOTORON signal is a logic low, the cassette motor is off, then the cassette output is sent to the sound circuit.

5.1.14 I/O Bus Port

The Model 4P Bus is designed to allow easy and convenient interfacing of I/O devices to the Model 4P. The I/O Bus supports all the signals necessary to implement a device compatible with the Z80s I/O structure.

Addresses:

A0 to A7 allow selection of up to 256* input and 256 output devices if external I/O is enabled.

*Ports 80H to 0FFH are reserved for System use.

Data:

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus is external I/O is enabled.

Control Lines:

1. M1* — Z80A signal specifying an M1 or Operation Code Fetch Cycle or with IOREQ*, it specifies an Interrupt acknowledge.

2. IN* — Z80A signal specifying than an input is in progress. Logic AND of IOREQ* and WR*.

3. OUT* — Z80A signal specifying that an output is in progress. Logic AND of IOREQ* and WR*.

4. IOREQ* — Z80A signal specifying that an input or output is in progress or with M1*, it specifies an interrupt acknowledge.

5. RESET* — system reset signal.

6. IOBUSINT* — input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled.

7. IOBUSWAIT* — input to the CPU wait line allowing I/O Bus device to force wait states on the Z80 if external I/O is enabled.

8. EXTIOSEL* — input to I/O Bus Port circuit which switches the I/O Bus data bus transceiver and allows and INPUT instruction to read I/O Bus data.

The address line, data line, and all control lines except RESET* are enabled only when the ENEXIO bit in port EC is set to one.

To enable I/O interrupts, the ENIOBUSINT bit in the PORT E0 (output port) must be a one. However, even if it is disabled from generating interrupts, the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port).

See Model 4P Port Bit assignments for port 0FF, 0EC, and 0E0.

Figure 5-16. Graphic Board Video Timing

The Model 4P CPU board is fully protected from "foreign I/O devices" in that all the I/O Bus signals are buffered and can be disabled under software control. To attach and use and I/O device on the I/O Bus, certain requirements (both hardware and software) must be met.

For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software. This will enable the data bus address lines and control signals to the I/O Bus edge connector. When the input device is selected, the hardware should acknowledge by asserting EXTIOSEL* low. This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines. See Figure 5-17 for the timing. EXTIOSEL* can be generated by NANDing IN and the I/O port address.

Output port device use is the same as the input port device in use, in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software — in the same fashion.

For either input or output devices, the IOBUSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU. Note that since dynamic memories are used in the Model 4P, the wait line should be used with caution. Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time. It is recommended that the IOBUSWAIT* line be held active no more than 500 μsec with a 25% duty cycle.

The Model 4P will support Z80 Mode 1 interrupts. A RAM jump table is supported by the LEVEL II BASIC ROMs image and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F. When an interrupt occurs, the program will be vectored to the user-supplied address if I/O Bus interrupts have been enabled. To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H.

5.1.15 FDC Circuit

The TRS-80 Model 4P Floppy Disk Interface provices a standard 5-1/4" floppy disk controller. The Floppy Disk Interface supports both single and double density encoding schemes. Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one. The amount of write precompensation is 250 nsec and is not adjustable. The data clock recovery logic incorporates a digital data separator which achieves state-of-the-art reliability. One or two drives may be controlled by the interface. All data transfers are accomplished by CPU data requests. In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip. The end of the data transfer is indicated by generation of a non-maskable interrupt from the interrupt request output of the FDC chip. A hardware watchdog timer insures that any error condition will not hang the wait line to the CPU for a period long enough to destroy RAM contents.

Input or Output Cycles.

*Inserted by Z80 CPU

Input or Output Cycles with Wait States.

*Inserted by Z80 CPU

†Coincident with IORQ* only on INPUT cycle.

Figure 5-17. I/O Bus Timing Diagram

Control and Data Buffering

The Floppy Disk Controller Board is an I/O port-mapped device which utilizes ports E4H, FØH, F1H, F2H, F3H, and F4H. The decoding logic is implemented on the CPU board. (Refer to Paragraph 5.1.5 Address Decoding for more information on Port Map). U31 is a bi-directional, 8-bit transceiver used to buffer data to and from the FDC and RS-232 circuits. The direction of data transfer is controlled by the combination of control signals DISKIN* and RS232IN*. If either signal is active (logic low), U31 is enabled to drive data onto the CPU data bus. If both signals are inactive (logic high), U31 is enabled to receive data from the CPU board data bus. A second buffer (U12) is used to buffer the FDC chip data to the FDC/RS232 Data Bus, (BD0-BD7), U12 is enabled all the time and it's direction controlled by DISKIN*. Again, if DISKIN* is active (logic low), data is enabled to drive from the FDC chip to the Main Data Busses. If DISKIN* is inactive (logic high), data is enabled to be transferred to the FDC chip.

Nonmaskable Interrupt Logic

Dual D flip-flop U100 (74LS74) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMIMASKREG*. The outputs of U100 enable the conditions which will generate a non-maskable interrupt to the CPU. The NMI interrupt conditions which are programmed by doing an OUT instruction to port E4H with the appropriate bits set. If data bit 7 is set, an FDC interrupt is enabled to generate an NMI interrupt. If data bit 7 is reset, interrupt requests request from the FDC are disabled. If data bit 6 is set, a Motor Time Out is enabled to generate an NMI interrupt. If data bit 6 is reset, interrupts on Motor Time Out are disabled. An IN instruction from port E4H enables the CPU to determine the source of the non-maskable interrupt. Data bit 7 indicates the status of FDC interrupt request (INTRQ) (0 = true, 1 = false). Data bit 6 indicates the status of Motor Time Out (0 = true, 1 = false). Data bit 5 indicates the status of the Reset signal (0 = true, 1 = false). The control signal RDNMISTATUS* gates this status onto the CPU data bus when active (logic low).

Drive Select Latch and Motor ON Logic

Selecting a drive prior to disk I/O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set. The following table describes the bit allocation of the Drive Select Latch:

Data Bit	Function
D0	Selects Drive 0 when set*
D1	Selects Drive 1 when set*
D2	Selects Drive 2 when set*
D3	Selects Drive 3 when set*
D4	Selects Side 0 when reset Selects Side 1 when set
D5	Write precompensation enabled when set, disabled when reset
D6	Generates WAIT if set
D7	Selects MFM mode if set Selects FM mode if reset

*Only one of these bits should be set per output

Hex D flip-flop U32 (74L174) latches the drive select bits, side select and FM*/MFM bits on the rising edge of the control signal DRVSEL*. A dual D flip-flop (U98) is used to latch the Wait Enable and Write precompensation enable bits on the rising edge of DRVSEL*. The rising edge of DRVSEL* also triggers a one-shot (1/2 of U54, 74LS123) which produces a Motor On to the disk drives. The duration of the Motor On signal is approximately three seconds. The spindle motors are not designed for continuous operation. Therefore, the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected. The Motor On one-shot is retriggerable by simply executing another OUT instruction to the Drive Select Latch.

Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an OUT to the Drive Select Latch with D6 set. Pin 5 of U98 will go high after this operation. This signal is inverted by 1/4th of U79 and is routed to the CPU where it forces the Z80A into a wait state. The Z80A will remain in the wait state as long as WAIT* is low. Once initiated, the WAIT* will remain low until one of five conditions is satisfied. One half of U77 (a five input NOR gate) is used to perform this function. INTQ, DRQ, RESET, CLRWAIT, and WAITIMOUT are the inputs to the NOR gate. If any one of these inputs is active (logic high), the output of the NOR gate (U77 pin 5) will go low. This output is tied to the clear input of the wait latch. When this signal goes low, it will clear the Q output (U98 pin 5) and set the Q* output (U98 pin 6). This condition causes WAIT* to go high which allows the Z80 to exit the wait state. U99 is a 12-bit binary counter which serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents. The counter is clocked by a 1 MHz clock and is enabled to count when its reset pin is low (U99 pin 11). A logic high on U99 pin 11 resets the counter outputs. U99 pin 15 is a divide-by-1024 output and is used to generate the signal WAITIMOUT. This watchdog timer logic will limit the duration of a wait to 1024μsec, even if the FDC chip should fail to generate a DRQ or an INTRQ.

If an OUT to Drive Select Latch is initiated with D6 reset (logic low), a WAIT is still generated. The 12-bit binary counter will count to 2 which will output CLRWAIT and clear the WAIT state. This allows the WAIT to occur only during the OUT instruction to prevent violating any Dynamic RAM parameters.

NOTE: This automatic WAIT will cause a 1-2 μsec wait each time an out to Drive Select Latch is performed.

Clock Generation Logic

A 4 MHz crystal oscillator and a 4-bit binary counter are used to generate the clock signals required by the FDC board. The 4 MHz oscillator is implemented with two inverters (1/3 of U39) and a quartz crystal (Y2). The output of the oscillator is inverted and buffered by 1/6 of U39 to generate a TTL level square wave signal. U37 is a 4-bit binary counter which is divided into a divide-by-2 and a divide-by-8 section. The divide-by-2 section is used to generate the 2 MHz output at pin 12. The 2 MHz is NANDed with 4MHz by 1/4 of U19 and the output is used to clock the divide-by-8 section of U37. A 1 MHz clock is generated at pin 9 of U37 which is 90° phase-shifted from the 2 MHz clock. This phase relationship is used to gate the guaranteed Write Data Pulse (WD) to the Write precompensation circuit. The 4 MHz is used to clock the digital data separator U18 and the Write precompensation shift register U55. The 1 MHz clock is used to drive the clock input of the FDC chip (U13) and the clock input of the watchdog timer (U99).

Disk Bus Output Drivers

High current open collector drivers U20 and U56 are used to buffer the output signals from the FDC circuit to the disk drives.

Write Precompensation and Write Data Pulse Shaping Logic

The Write Precompensation logic is comprised of U55 (74LS195), 1/4 of U19 (74LS00), 1/4 of U74 (74LS04), and 1/2 of U77 (74LS260). U55 is a parallel in, serial out shift register and is clocked by 4 MHz which generates a precompensation value of 250 nsec. The output signals EARLY and LATE of the FDC chip (U13) are input to P0 and P2 of the shift register. A third signal is generated by 1/4 of U75 when neither EARLY nor LATE is active low and is input to P1 of U55. WD of the FDC chip is NANDed with 2 MHz to gate the guaranteed Write Data Pulse to U55 for the parallel load signal SHFT/LD. When U55 pin 9 is active low, the signals preset at P1-P3 are clocked in on the rising edge of the 4 MHz clock. After U55 pin 9 goes high, the data is shifted out at a 250 nsec rate. EARLY will generate a 250 nsec delay, NOT EARLY AND NOT LATE will generate a 500 nsec delay, and LATE will generate a 750 nsec delay. This provides the necessary precompensation for the write data. As mentioned previously, Write Precompensation is enabled through software by an OUT to the Drive Select Latch with bit 5 set. This sets the Q output of the 74LS74 (U98 pin 9) which is ANDed with DDEN which disables the shift register U55. DDEN disables Write Precompensation in the single density mode. The resulting signal also enables U75 to allow the write data (WD) to bypass the Write Precompensation circuit. The Write Data (WD) pulse is shaped by a one-shot (1/2 of U54) which stretches the data pulses to approximately 500 nsec.

Figure 5-18. Write Precompensation Timing

Clock and Read Data Recovery Logic

The Clock and Read Data Recovery Logic is comprised of one chip U18 (FDC9216). The FDC9216 is a Floppy Disk Data Separator (FDDS) which converts a single stream of pulses from the disk drive into separate clock and data pulses for input to the FDC chip. The FDDS consists of a clock divider, a long-term timing corrector, a short-time timing corrector and reclocking circuitry. The reference clock (REFCLK) is a 4 MHz and is divided by the internal clock divider. CD0 and CD1 of the FDDS chip control the divisor which divides REFCLK. With DC1 grounded (logic low), CD0 (when a logic low) generates a divide-by-1 for MFM mode and when logic high generates a divide-by-2 for FM mode. CD0 is controlled by the signal DDEN* which is Double Density enable or MFM enable. The FDDS detects the leading edges of RD* pulses and adjusts the phase of the internal clock to generate the separated clock (SEPCLK) to the FDC chip. The separate long and short term timing correctors assure the clock separation to be accurate. The separated Data (SEPD*) is used as the RDD* input to the FDC chip.

Floppy Disk Controller Chip

The 1793 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation. The following port addresses are assigned to the internal registers of the 1793 FDC chip:

Port No.	Function
F0H	Command/Status Register
F1H	Track Register
F2H	Sector Register
F3H	Data Register

5.1.16 RS-232-C Circuit

RS-232C Technical Description

The RS-232C circuit for the Model 4P computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input-output interface connector (J4). The heart of the circuit is the TR1865 Asynchronous Receiver/Transmitter U30. It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop, and parity bits. For a more detailed description of how this LSI circuit performs these functions, refer to the TR1865 data sheets and application notes. The transmit and receive clock rates that the TR1865 needs are supplied by the Baud Rate Generator U52 (BR1941L) or (BR1943). This circuit takes the 5.0688 MHz supplied by the system timing circuit and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks. The rates available from the BRG go from 50 Baud to 19200 Baud. See the BRG table for the complete list.

BRG Programming Table

Nibble Loaded	Transmit/ Receive Baud Rate	16X Clock	Supported by SETCOM
0H	50	0.8 kHz	Yes
1H	75	1.2 kHz	Yes
2H	110	1.76 kHz	Yes
3H	134.5	2.1523 kHz	Yes
4H	150	2.4 kHz	Yes
5H	300	4.8 kHz	Yes
6H	600	9.6 kHz	Yes
7H	1200	19.2 kHz	Yes
8H	1800	28.8 kHz	Yes
9H	2000	32.081 kHz	Yes
AH	2400	38.4 kHz	Yes
BH	3600	57.6 kHz	Yes
CH	4800	76.8 kHz	Yes
DH	7200	115.2 kHz	Yes
EH	9600	153.6 kHz	Yes
FH	19200	307.2 kHz	Yes

The RS-232C circuit is port mapped and the ports used are E8 to EB. Following is a description of each port on both input and output.

Port	Input	Output
E8	Modem status	Master Reset, enables UART control register load
EA	UART status	UART control register load and modem control
E9	Not Used	Baud rate register load enable bit
EB	Receiver Holding register	Transmitter Holding register

Interrupts are supported in the RS-232C circuit by the Interrupt mask register (U92) and the Status register (U44) which allow the CPU to see which kind of interrupt has occurred. Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors — parity, framing, or data overrun. This allows a minimum of CPU overhead in transferring data to or from the UART. The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read). Refer to the IO Port description for a full breakdown of all interrupts and their bit positions.

All Model I, III, and 4 software written for the RS-232-C interface is compatible with the Model 4P RS-232-C circuit, provided the software does not use the sense switches to configure the interface. The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface . The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145).

Pinout Listing

The following list is a pinout description of the DB-25 connector (P1).

Pin No.	Signal
1	PGND (Protective Ground)
2	TD (Transmit Data)
3	RD (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear To Send)
6	DSR (Data Set Ready)
7	SGND (Signal Ground)
8	CD (Carrier Detect)
19	SRTS (Spare Request to Send)
20	DTR (Data Terminal Ready)
22	RI (Ring Indicate)

5.1.17 CPU Board Troubleshooting Guide

This section is a general guide for service personnel to check out and troubleshoot the Model 4P Main Logic CPU Board. Procedures in section 4 Troubleshooting should be followed before proceeding to following steps. This guide will provide step by step procedures to help isolate the faulty area on the CPU board. Knowledge of each area of the CPU board is necessary to determine exact component failure. Refer of CPU Board Schematics and Theory of Operation during troubleshooting for specific check points and testing.

1. No video messages are displayed and correct data does not appear at video output connector J9.
   If above condition exists, go to 2; if video okay, but Model 4P does not boot properly, go to 10.
   If video and boot-up is okay, go to 15.

2. Check for video timing signals 12M and 10M and input of U127.
   If okay, go to 3; if one or both bad, go to 7.

3. Check for proper timing signals output from U127 (SHIFT*, XADR7*, CRTCLK, POT*, LOAD*, LOADS*, DCLK).
   If okay, then go to 4; if one or more bad, replace U127 or U128.

4. Check if 68046 U85 is working properly and has correct input signals.
   If all okay, then go to 5. If bad, replace U85 or check for input signals where they originate.

5. Check for timing and proper signals at U82 and U42.
   If bad, replace as necessary; if okay, go to 6.

6. Check shift register and repair.

7. Check for 20M output of Y1 pin 8.
   If okay, go to 8; if bad, replace Y1.

8. Check for outputs of U126 (PCLK, RS232CLK, and 10M).
   If okay, then go to 9; if any bad, replace U126.

9. Check for 12M at output of U148 pin 9.
   If okay, then video should work; if bad, check U147, U148, and U149 and replace if necessary.

10. Run Memory Test in Boot ROM by holding down period (.) and toggling Reset.
    If memory checks okay, then go to 11; if not, check memory circuit and/or replace RAM chips.

11. Check Clock circuit of Floppy Disk Controller.
    If 4MHz, 2MH, and 1MHz okay, go to 12; if bad, repair or replace necessary components.

12. Check for all incoming signals to the FDC chip U13.
    If any bad, repair as necessary; if okay, go to 13.

13. Check all handshaking signals to FDC chip from CPU.
    If okay, go to 14; if bad, repair as necessary.

14. Check Data Bus and control lines.
    If okay, then problem still exists in Floppy Disk Circuit or Floppy Disk Drive. Refer to each section accordingly. If bad, replace as necessary.

15. If unit boots okay, then boot Model 4P Diagnostics Diskette and execute each diagnostic to isolate any minor problems on CPU Board.

1. ALL RESISTANCE VALUES ARE IN OHMS, K=1000.

NOTE (UNLESS OTHERWISE SPECIFIED):

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DRAWING NO.	REV
8000192	A
SCALE N/A	SHEET 2 OF 7

DRAWING NO.	REV
8000192	A
SCALE N/A	SHEET 3 OF 7

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D0-D7
LPOUT*
U1 LS123
U2 LS374
U3 LS244
U21 LS04
DATA STROBE*
J1 LINE PRINTER (34 PIN EDGE CARD CONN.)
LPRD*
RP2 1.5K
U58 LS240
KEYBD*
J6 KEYBOARD
A0-A7
J7 GRAPHICS BOARD (34 PIN HEADER)
CASSOUT*
CASSMOTORON
SEN*
IOREQ*
U142 LS02
U130 LS74
R39 3.6K
R40 1.8K
Q2 2N3906
R38 120Ω
C159 1µF
B1 TRANSDUCER OMB-06
FAST
VSYNC
U22 LS74
U62 S32
U25 LS38
RTCIN
INT*
ENRTC
GSEL0*
GSEL1*
IORQ*
CL166*
GEN*
8064*
8064
U23 LS00
U24 LS02
R11 4.7K
J3 INTERNAL I/O BUS (50 PIN HEADER)
U7 LS245
EXTIOSEL*
R7 150Ω
U9 LS244
U10 LS367
U6 LS04
ENEXTIO
WAIT*
IOBUSWAIT*
IOBUSINT*
ENIOBUSINT
IOBUSINT
R5 150Ω
R6 150Ω
J2 EXTERNAL I/O BUS (50 PIN EDGE CARD CONN.)
PROPRIETARY INFORMATION
DRAWING NO. 8000192
REV A
SCALE N/A
SHEET 5 OF 7

U31 LS245
U23 LS08
U72 LS368
U2 LS245
U3 1793
U18 9216
U55 LS95
U54 LS123
U32 LS174
U98 LS74
U100 LS74
U3 40408
U37 LS93
U19 LS00
U39 LS04
U56 7416
U20 7416
U79 LS38
U78 LS08
U77 LS260
U75 LS02
U74 LS04
U9 LS00
J5 FLOPPY DISK (34 PIN HEADER)
PROPRIETARY INFORMATION
DRAWING NO. 8000192
REV A
SCALE
SHEET 6 OF 7

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DRAWING NO.	REV
8000192	A
SCALE N/A	SHEET 7 OF 7

FRONT SILKSCREEN
8709427 REV A
TANDY CORP
8709427 REV A
1700254
JIO POWER
VIDEO
RESET
325.4
350.8
TANDY 15-AUG-83 TAN02H
GESSCO

FRONT
8709427 REV A TANDY CORP
325.4
358.8
TANDY 15 Aug-83 TAN02H
GE55L1 PHO=1 SEG=1 V10-0

TANDY CORP 8709427 REV A
REAR
8709427 REV A
1700254
TANDY CORP.
1983 MADE IN USA
350.8
325.4
TAN02H 15-Aug-83 TANDY
VIA=0 SEG=0 PAD=0 GE.SSI 0

Parts List

Main PCB Assembly, Model 4P Computer

Item	Sym	Description	Part Number
1	1	PCB, Main Logic	87Ø9427
2	21	Staking Pin	8529Ø14
3	1	Socket, 8-Pin DIP (U79)	85Ø9Ø11
4	16	Socket, 16-Pin DIP (U115-13Ø)	85Ø9ØØ3
5	1	Socket, 18-Pin DIP (U76)	85Ø9ØØ6
6	1Ø	Socket, 2Ø-Pin DIP (U39-41, 47,5Ø,51,62,63,84,11Ø)	85Ø9ØØ9
7	3	Socket, 24-Pin DIP (U16,24,44)	85Ø9ØØ1
8	4	Socket, 4Ø-Pin DIP (U26,43, U72,81)	85Ø9ØØ2
9	1	Connector, 4-Pin (J8)	8519219
1Ø	1	Connector, 3-Pin (J1Ø)	
11	1	Connector, 6-Pin (J9)	8519211
12	1	Connector, Dual 8 (J6)	8519184
13	1	Connector, 34-Pin (J5)	
14	1	Connector, 34-Pin (J7)	
15	1	Connector, 25-Pin (J4)	8519199
	B1	Transducer, Sound	849ØØØ3
	C1 thru C11	Capacitor, .1 mfd, 5ØV Mono Axial	8374194
	C13	Capacitor, .1 mfd, 5ØV Mono Axial	8374194
	C15 thru C2Ø	Capacitor, .1 mfd, 5ØV Mono Axial	8374194
	C22 thru C48	Capacitor, .1 mfd, 5ØV Mono Axial	8374194
	C5Ø thru C64	Capacitor, .1 mfd, 5ØV Mono Axial	8374194
	C66 thru C88	Capacitor, .1 mfd, 5ØV Mono Axial	8374194
	C9Ø thru C13Ø	Capacitor, .1 mfd, 5ØV Mono Axial	8374194

Parts List

Main PCB Assembly, Model 4P Computer

Item	Sym	Description	Part Number
	C131 thru C138	Capacitor, 22 mfd, 16V Elec Radial	8326221
	C139	Capacitor, 1ØØØ pfd, 5ØV Cer Disk	83Ø21Ø4
	C14Ø	Capacitor, .Ø22 mfd, 5ØV Cer Disk	83Ø3224
	C141	Capacitor, .Ø22 mfd, 5ØV Cer Disk	83Ø3224
	C142	Capacitor, 33 pfd, 5ØV Cer Disk	83ØØ334
	C143	Capacitor, 15ØØ pfd, 5ØV Cer Disk	
	C144	Capacitor, 15ØØ pfd, 5ØV Cer Disk	
	C145	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C146	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C148	Capacitor, 9-35 mfd, Trimmer	
	C149	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C15Ø thru C152	Capacitor, 18Ø pfd, 5ØV C.Disk Z5U	83Ø1184
	C153	Capacitor, 1ØØ pfd, 5ØV Cer Disk	83Ø11Ø4
	C154	Capacitor, 47Ø pfd, 5ØV Cer Disk	83Ø1474
	C155	Capacitor, 18Ø pfd, 5ØV Cer Disk Z5U	83Ø1184
	C156	Capacitor, 1ØØ pfd, 5ØV Cer Disk	83Ø11Ø4
	C157	Capacitor, 33 mfd, 16V Elec Radial	8326331
	C158	Capacitor, 2ØØ pfd, 5ØV Cer Disk Z5U	83Ø1223
	C159	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C161	Capacitor, 1Ø mfd, 16V Elec Radial	8326lØ1
	C162	Capacitor, 1Ø mfd, 16V Elec Radial	8326lØ1
	C166	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C172	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C176	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C181	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C2ØØ	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C2Ø1	Capacitor, 22 mfd, 16V Elec Radial	8326221
	C2Ø2	Capacitor, 1Ø mfd, 16V Elec Radial	8326lØ1
	C2Ø3	Capacitor, .1 mfd, 5ØV Mono Axial	8374lØ4
	C2Ø4	Capacitor, 1Ø mfd, 16V Elec Radial	8326lØ1
	C2Ø5	Capacitor, 1ØØ pfd, 5ØV Cer Disk	83Ø11Ø4
	CR1	Diode, 1N4148	815Ø148
	Q1	Transistor, 2N39Ø6	81ØØ9Ø6
	Q2	Transistor, 2N39Ø6	81ØØ9Ø6

Parts List

Main PCB Assembly, Model 4P Computer

Item	Sym	Description	Part Number
	R1	Resistor, 75Ø ohm, 1/4W 5%	82Ø7175
	R2	Resistor, 1ØØ kohm, 1/4W 5%	82Ø741Ø
	R3 thru R5	Resistor, 4.7 kohm, 1/4W 5%	82Ø7247
	R6	Resistor, 22 ohm, 1/4W 5%	82Ø7Ø22
	R7	Resistor, 22Ø ohm, 1/4W 5%	82Ø7122
	R8	Resistor, 1.2 kohm, 1/4W 5%	82Ø7212
	R9	Resistor, 2.2 kohm, 1/4W 5%	82Ø7222
	R11	Resistor, 1ØØ ohm, 1/4W 5%	82Ø711Ø
	R12	Resistor, 13Ø ohm, 1/4W 5%	82Ø7113
	R13	Resistor, 13Ø ohm, 1/4W 5%	82Ø7113
	R14	Resistor, 1 kohm, 1/4W 5%	82Ø721Ø
	R15	Resistor, 1 kohm, 1/4W 5%	82Ø721Ø
	R16	Resistor, 3 kohm, 1/4W 5%	82Ø723Ø
	R17	Resistor, 82Ø ohm, 1/4W 5%	82Ø7182
	R18	Resistor, 2ØØ ohm, 1/4W 5%	82Ø712Ø
	R19	Resistor, 16Ø kohm, 1/4W 5%	82Ø7416
	R2Ø thru 23	Resistor, 27 ohm, 1/4W 5%	82Ø7Ø27
	R24	Resistor, 91Ø ohm, 1/4W 5%	82Ø7191
	R25	Resistor, 91Ø ohm, 1/4W 5%	82Ø7191
	R26	Resistor, 15Ø ohm, 1/4W 5%	82Ø7115
	R27	Resistor, 1Ø kohm, 1/4W 5%	82Ø731Ø
	R28	Resistor, 1Ø kohm, 1/4W 5%	82Ø731Ø
	R29	Resistor, 27Ø kohm, 1/4W 5%	82Ø7427
	R3Ø	Resistor, 2Ø kohm, 1/4W 5%	82Ø732Ø
	R31 thru R33	Resistor, 4.7 kohm, 1/4W 5%	82Ø7247
	R34	Resistor, 3.6 kohm, 1/4W 5%	82Ø7236
	R36	Resistor, 12Ø ohm, 1/4W 5%	82Ø7112
	R37 thru R39	Resistor, 15Ø ohm, 1/4W 5%	82Ø7115
	R42	Resistor, 4.7 kohm, 1/4W 5%	82Ø7247
	R43	Resistor, 1Ø kohm, 1/4W 5%	82Ø731Ø
	R44 thru 46	Resistor,	
	RP1	Resistor Pak 27 ohm, 16-Pin DIP	829ØØ27
	RP2	Resistor Pak 1.5 kohm, 1Ø-Pin SIP	829ØØ15
	RP3	Resistor Pak 15Ø ohm, 1Ø-Pin SIP	829ØØ13

Parts List

Main PCB Assembly, Model 4P Computer

Item	Sym	Description	Part Number
	U1	IC, 74LS123, Multivibrator	8Ø2Ø123
	U2	IC, 74LS374, Flip Flop	8Ø2Ø374
	U3	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U4	IC, 74LS38, Quad 2-Input NAND	8Ø2ØØ38
	U5	IC, 74LSØ8, Quad 2-Input AND	8Ø2ØØØ8
	U6	IC, 74LSØ4, Hex Inverter	8Ø2ØØØ4
	U7	IC, 74LS245, Transceiver	8Ø2Ø245
	U8	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U9	IC, 74LS367, Hex Driver	8Ø2Ø367
	U1Ø	IC, 74LSØ4, Hex Inverter	8Ø2ØØØ4
	U11	IC, 74LS74, Flip Flop	8Ø2ØØ74
	U13	IC, 74LSØ2, 2-Input NOR	8Ø2ØØØ2
	U15	IC, 74S32, Quad 2-Input OR	8Ø1ØØ32
	U16	IC, MCM68A316E, Character ROM	8Ø49ØØ7
	U17	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U18	IC, 74SLS166, 8-Bit Shift Reg	8Ø2Ø166
	U19	IC, 74LS175, Quad Flip Flop	8Ø2Ø175
	U2Ø	IC, 74SØ4, Hex Inverter	8Ø1ØØØ4
	U22	IC, 74LS153, Multiplexer	8Ø2Ø153
	U23	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U24	IC, 4Ø16, 2K x 8 RAM Static	8Ø4Ø116
	U25	IC, 74LS157, Multiplexer	8Ø2Ø157
	U26	IC, 68Ø45, CRTC	8Ø4ØØ45
	U27	IC, 74LS273, Flip Flop	8Ø2Ø273
	U28	IC, 74LS373, Octal Latch	8Ø2Ø373
	U29	IC, 74LS157, Multiplexer	8Ø2Ø157
	U3Ø	IC, 74LS14, Hex Inverter	8Ø2ØØ14
	U31	IC, 74LSØ2, 2-Input NOR	8Ø2ØØØ2
	U32	IC, 74LSØ8, Quad 2-Input AND	8Ø2ØØØ8
	U33	IC, 74LSØØ, Quad 2-Input NAND	8Ø2ØØØØ
	U34	IC, 74LS157, Multiplexer	8Ø2Ø157
	U35	IC, 74LS51, AND-OR Inverter	8Ø2ØØ51
	U36	IC, 74LSØØ, Quad 2-Input NAND	8Ø2ØØØØ
	U37	IC, 74LS86, Quad 2-Input OR	8Ø2ØØ86
	U38	IC, 74LS368, Hex Driver	8Ø2Ø368
	U39	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U4Ø	IC, 74LS245, Transceiver	8Ø2Ø245
	U41	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U42	IC, 74FØ4, Hex Inverter	8Ø15ØØ4
	U43	IC, Z8ØA, CPU	8Ø4788Ø
	U44	IC, MCM68A322, Boot ROM	
	U45	IC, 74LS138, 1 of 8 Demultiplexer	8Ø2Ø138
	U46	IC, 74LS138, 1 of 8 Demultiplexer	8Ø2Ø138

Parts List

Main PCB Assembly, Model 4P Computer

Item	Sym	Description	Part Number
	U47	IC, PAL1ØL8, Control Decode	8Ø756Ø8
	U48	IC, 74LS9Ø, Counter	8Ø2ØØ9Ø
	U5Ø	IC, PAL16R6A, System Timing	8Ø75Ø66
	U51	IC, PAL1ØL8, Video Timing	8Ø757Ø8
	U52	IC, NE564, PLL/VCO	8Ø4Ø564
	U53	IC, 74LSØ4, Binary Counter	8Ø2ØØØ4
	U54	IC, 74LS161, Counter	8Ø2Ø161
	U55	IC, 74LS138, 1 of 8 Demultiplexer	8Ø2Ø138
	U56	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U57	IC, 74LS174, Flip Flop	8Ø2Ø174
	U58	IC, 74LS273, Flip Flop	8Ø2Ø273
	U59	IC, 74LS174, Flip Flop	8Ø2Ø174
	U6Ø	IC, 74LS74, Flip Flop	8Ø2ØØ74
	U62	IC, PAL16L8, Memory Map	8Ø75668
	U63	IC, PAL16L8, Page Map	8Ø75568
	U64	IC, 74LS32, Quad 2-Input OR	8Ø2ØØ32
	U66	IC, 1488, Driver	8Ø5Ø188
	U67	IC, 1489, Receiver	8Ø5Ø189
	U68	IC, 1489, Receiver	8Ø5Ø189
	U69	IC, 74LS244, Octal Buffer	8Ø2Ø244
	U7Ø	IC, 74LS367, Hex Driver	8Ø2Ø367
	U71	IC, 74LS27, Triple 3-Input NOR	8Ø2ØØ27
	U72	IC, TR1865, UART	8Ø4Ø865
	U73	IC, 74LS174, Flip Flop	8Ø2Ø174
	U74	IC, 74LS367, Hex Driver	8Ø2Ø367
	U75	IC, 74LS139, 1 of 4 Demultiplexer	8Ø2Ø139
	U76	IC, BR1943-ØØ, Clock Generator	8Ø4Ø943
	U77	IC, 74LS38, Quad 2-Input NAND	8Ø2ØØ38
	U78	IC, 74LSØ4, Hex Inverter	8Ø2ØØØ4
	U79	IC, FDC9216	8Ø4Ø216
	U8Ø	IC, 74LS245, Transceiver	8Ø2Ø245
	U81	IC, WD1793	8Ø3Ø793
	U82	IC, 74LS26Ø, 5-Input NOR	8Ø2Ø26Ø
	U83	IC, 7416, Hex Inverter	8ØØØØ16
	U84	IC, 74LS245, Transceiver	8Ø2Ø245
	U85	IC, 74LSØ2, 2-Input NOR	8Ø2ØØØ2
	U86	IC, 74LS174, Flip Flop	8Ø2Ø174
	U87	IC, 74LSØ4, Hex Inverter	8Ø2ØØØ4
	U88	IC, 74LS368, Hex Driver	8Ø2Ø368
	U9Ø	IC, 74LS38, Quad 2-Input NAND	8Ø2ØØ38
	U91	IC, 7416, Hex Inverter	8ØØØØ16
	U92	IC, 74LS93, Binary Counter	8Ø2ØØ93
	U93	IC, 7416, Hex Inverter	8ØØØØ16
	U94	IC, 74LSØ8, Quad 2-Input AND	8Ø2ØØØ8

Parts List

Main PCB Assembly, Model 4P Computer

Item	Sym	Description	Part Number
	U95	IC, 74LSØ4, Hex Inverter	8Ø2ØØØ4
	U96	IC, 74LSØØ, Quad 2-Input NAND	8Ø2ØØØØ
	U97	IC, 74LS74, Flip Flop	8Ø2ØØ74
	U98	IC, 74LSØØ, Quad 2-Input NAND	8Ø2ØØØØ
	U99	IC, 74LS195, Shift Register	8Ø2Ø195
	U1ØØ	IC, 74LS24Ø, Octal Buffer	8Ø2Ø24Ø
	U1Ø1	IC, 74LS32, Quad 2-Input OR	8Ø2ØØ32
	U1Ø2	IC, 74LS74, Flip Flop	8Ø2ØØ74
	U1Ø4	IC, Delay Line	8429Ø2Ø
	U1Ø5	IC, 74LS74, Flip Flop	8Ø2ØØ74
	U1Ø6	IC, MC14Ø4Ø, Binary Counter	8Ø3ØØ4Ø
	U1Ø7	IC, 74LS123, Multivibrator	8Ø2Ø123
	U1Ø8	IC, 74LS157, Multiplexer	8Ø2Ø157
	U1Ø9	IC, 74LS157, Multiplexer	8Ø2Ø157
	U11Ø	IC, 74LS245, Transceiver	8Ø2Ø245
	U111	IC, 74S64, AND-OR Inverter	8Ø1ØØ64
	U112	IC, 74S32, Quad 2-Input OR	8Ø1ØØ32
	U113	IC, 74S112, J-K Flip Flop	8Ø1Ø112
	U114	IC, 74FØ8, Quad 2-Input AND	8Ø15ØØ8
	U115 thru U13Ø	IC, MCM6665, 64K DRAM, 2ØØ nsec	8Ø4Ø665
	U131	IC, 74LS283, Binary Adder	8Ø2Ø283
	U161	IC, 74LS11, Triple 3-Input AND	8Ø2ØØ11
	Y1	Crystal, 2Ø.2752 MHz	84Ø9Ø32
	Y2	Crystal, 4 MHz	84Ø9Ø1Ø

4P GATE ARRAY THEORY OF OPERATION

5.2 CPU THEORY OF OPERATION

5.2.1 Introduction

Contained in the following paragraphs is a description of the component parts of the Model 4P CPU Gate Array. It is divided into the logical operational functions of the computer. All components are located on the Main CPU board inside the case housing. Refer to Section 3 for disassembly/assembly procedures.

5.2.2 Reset Circuit

The Model 4P reset circuit provides the neccessary reset pulses to all circuits during power up and reset operations. R25 and C214 provide a time constant which holds the input of U121 low during power-up. This allows power to be stable to all circuits before the RESET* and RESET signals are applied. When C214 charges to a logic high, the output of U121 triggers the input of a retriggerable one-shot multivibrator (U1). U1 outputs a pulse with an approximate width of 70 microsecs. When the reset switch is pressed on the front panel, this discharges C214 and holds the input of U121 low until the switch is released. On release of the switch, C214 again charges up, triggering U121 and U1 to reset the microcomputer. Another signal POWRST* is generated to clear drive select circuit immediately when reset switch is pressed.

5.2.3 CPU

The central processing unit (CPU) of the Model 4P microcomputer is a Z80A microprocessor. The Z80A is capable of running in either 2 MHz or 4 MHz mode. The CPU controls all functions of the microcomputer through use of its address lines (A0-A15), data lines (D0-D7), and control lines (/M1, /IOREQ, /RD, /WR, /MREQ, and /RFSH). The address lines (A0-A15) are buffered to other ICs through two 74LS244s (U67 and U27) which are enabled all the time with their enables pulled to GND. The control lines are buffered to other ICs through a 74F04 (U87). The data lines (D0-D7) are buffered through a bi-directional 74LS245 (U86) which is enabled by BUSEN* and the direction is controlled by BUSDIR*.

5.2.4 System Timing

The main timing reference of the microcomputer, with the exception of the FDC circuit, is generated by a Gate Array U148 and a 20.2752 MHz Crystal. This reference is internally divided in the Gate Array to generate all necessary timing for the CPU, video circuit, and RS-232-C circuit. The CPU clock is generated U148 which can be either 2 or 4MHz depending on the logic state of FAST input (pin 6 of U148). If FAST is a logic low, the U148 generates a 2.02752 MHz clock. If FAST is a logic high, U148 generates a 4.05504 MHz signal. PCLK (pin 23 of U148) is filtered through a ferrite bead (FB2) and 22Ω Resistor (R9) and then fed to the CPU U45. PCLK is generated as a symmetrical clock and is never allowed to be short cycled. (eg.) Not allowed to generate a low or high pulse under 110 nanoseconds.

5.2.4.1 Video Timing

The video timing is also generated by U148 with the help of a PLL Multiplier Module (PMM) U146. These two ICs generate all the necessary timing signals for the four video modes: 64 x 16, 32 x 16, 80 x 24, and 40 x 24. Two reference clocks are required for the four video modes. One reference clock is 10.1376 MHz. It is generated internally to U148, and is used by the 64 x 16 and 32 x 16 modes. The second reference clock is a 12.672 MHz (12M) clock which is generated by the PMM U146. 12M clock is used by the 80 x 24 and 40 x 24 modes. A 1.2672 MHz (1.2M16) signal is output from pin 3 of U148 and is generated from the master reference clock, the 20.2752 MHz crystal. 1.2M16 is used for a reference clock for the PMM. The PMM is internally set to oscillate at 12.672 MHz which is output as 12M. U148 divides 12M by 10 to generate a second 1.2672 MHz clock (1.2M10) which is fed into pin 5 of U146 (PMM). The two 1.2672 MHz signals are internally compared in the PMM where it corrects the 12.672 MHz output so it is synchronized with the 20.2752 MHz clock.

MODSEL and 8064* signals are used to select the desired video mode. 8064* controls which reference clock is used by U127 and MODSEL controls the single or double character width mode. Refer to the following chart for selecting each video mode.

8064*	MODSEL	Video Mode
0	0	64 x 16
0	1	32 x 16
1	0	80 x 24
1	1	40 x 24

*This is the state to be written to latch U85. Signal is inverted before being input to U148.

Figure 5-19. Model 4P Functional Block Diagram

DCLK, the reference clock selected, is output from U148. U148 generates SHIFT*, XADR7*, CRTCLK, LOADS*, and LOAD* for proper timing for the four video modes. U149 also generated H, I, and J which are fed to the Graphics Port J7 for reference timings of Hires graphics video. Refer to Video Timing, Figs. 5-3 and 5-4 for timing reference.

5.2.5 Address Decode

The Address Decode section will be divided into two subsections: Memory Map decoding and Port Map decoding.

5.2.5.1 Memory Map Decoding

Memory Map Decoding is accomplished by Gate Array 4.2 (U106). Four memory map modes are available which are compatible with the Model III and Model 4 microcomputers. U106 is used for memory map control which also controls page mapping of the 32K RAM pages. Refer to Memory Maps below.

5.2.5.2 Port Map Decoding

Port Map Decoding is accomplished by Gate Array 4.2 (U106). U106 decodes the low order address (A0-A7) from the CPU and decodes the port being selected. The IN* signal allows the CPU to read from a selected port and the OUT* signal allows the CPU to write to the selected port. Refer to IO Port Assignment.

5.2.6 ROM

The Model 4P contains only a 4K x 8 Boot ROM (U69). This ROM is used only to boot up a Disk Operating System into the RAM memory. If Model III operation or DOS is required, then the RAM from location 0000-37FFH must be loaded with an image of the Model III or 4 ROM code and then executed. A system program called MODEL A/III is supplied with the Model 4P to provide the ROM image for proper Model III operation. On power-up, the Boot ROM is selected and mapped into location 0000-0FFFH. If the Boot ROM is not required after boot up, the Boot ROM must be mapped out by OUTing to port 9CH with D0 set or by selecting Memory Map modes 2 or 3. In Mode 1 the RAM is write enabled for the full 14K. This allows the RAM area mapped where Boot ROM is located to be written to while executing out of the Boot ROM. Refer to Memory Maps.

The Model 4P Boot ROM contains all the code necessary to initialize hardware, detect options selected from the keyboard, read a sector from a hard disk or floppy, and load a copy of the Model III ROM-Image (as mentioned) into the lower 14K of RAM.

The firmware is divided into the following routines:

* Hardware Initialization
* Keyboard Scanner
* Control
* Floppy and Hard Disk Driver
* Disk Directory Searcher
* File Loader
* Error Handler and Displayer
* RS-232 Boot
* Diagnostic Package

Theory of Operation

This section describes the operation of various routines in the ROM. Normally, the ROM is not addressable by normal use. However, there are several routines that are available through fixed calling locations and these may be used by operating systems that are booting.

On a power-up or RESET condition, the Z80's program counter is set to address 0 and the boot ROM is switched-in. The memory map of the system is set to Mode 0. (See Memory Map for details.) This will cause the Z80 to fetch instructions from the boot ROM.

The Initialization section of the Boot ROM now performs these functions:

1. Disables maskable and non-maskable interrupts
2. Interrupt mode 1 is selected
3. Programs the CRT Controller
4. Initializes the boot ROM control areas in RAM.
5. Sets up a stack pointer
6. Issues a Force Interrupt to the Floppy Disk Controller to abort any current activity
7. Sets the system clock to 4mhz
8. Sets the screen to 64 x 16
9. Disables reverse video and the alternate character sets
10. Tests for < . > key being pressed*
11. Clears all 2K of video memory

* This is a special test. If the < . > is being pressed, then control is transferred to the diagnostic package in the ROM. All other keys are scanned via the Keyboard Scanner.

Figure 5-20. Video Timing 64 x 16 Mode 80 x 24 Mode

Figure 5-21. Video Timing 32 x 16 Mode 40 x 24 Mode

The Keyboard scanner is now called. It scans the keyboard for a set period of time and returns several parameters based on which, if any, keys were pressed.

The keyboard scanner checks for several different groups of keys. These are shown below:

Function Group	Selection Group
<F1>	A
<F2>	B
<F3>	C
<1>	D
<2>	E
<3>	F
<Left-Shift>	G
<Right-Shift>	
<Ctrl>	
<Caps>	

Special Keys	Misc Keys
<P>	<Enter>
<L>	<Break>
<N>	

When any key in the Function Group is pressed, it is recorded in RAM and will be used by the Control routine in directing the action of the boot. If more than one of these keys are pressed during the keyboard scan, the last one detected will be the one that is used. The Function group keys are currently defined as:

<F1> or <1>	Will cause hard disk boot
<F2> or <2>	Will cause floppy disk boot
<F3> or <3>	Will force Model III mode
<Left-Shift>	Reserved for future use
<Right-Shift>	Boot from RS-232 port
<Ctrl>	Reserved for future use
<Caps>	Reserved for future use

The Special keys are commands to the Control routine which direct handling of the Model III ROM-image. Each key is detected individually.

<P>	When loading the Model III ROM-image, the user will be prompted when the disks can be switched or when ROM BASIC can be entered by pressing <Break>.
<N>	Instructs the Control routine to not load the Model III ROM-image, even if it appears that the operating system being booted requires it.
<L>	Instructs the Control routine to load the Model III ROM-image, even if it is already loaded. This is useful if the ROM-image has been corrupted or when switching ROM-images. (Note that this will not cause the ROM-image to be loaded if the boot sector check indicates that the Model III ROM image is not needed. Press <F3> or <F3> and <L> to accomplish that.

The Selection group keys are used in determining which file will be read from disk when the ROM-image is loaded. For details of this operation, see the Disk Directory Searcher. If more than one of the Selection group keys are pressed, the last one detected will be the one that is used.

The Miscellaneous keys are:

<Break>	Pressing this key is simply recorded by setting location 405BH non-zero. It is up to an operating system to use this flag if desired.
<Enter>	Terminates the Keyboard routine. Any other keys pressed up to that time will be acted upon. <Enter> is useful for experienced users who do not want to wait until the keyboard timer expires.

The Control section now takes over and follows the following flowchart.

Begin
<F1> or <1> pressed ?
Yes
1
Goto [1] (Hard Disk Boot)
No
<F2> or <2> pressed ?
Yes
2
Goto [2] (Floppy Disk Boot)
No
<F3> or <3> pressed ?
Yes
3
Goto [3] (Model III Boot)
No
<Right- Shift> pressed ?
Yes
4
Goto [4] (RS-232 Boot)
No
At this point, no valid Function keys have been pressed.
ARCNET Controller Board Present ?
Yes
Display an error message. (ARCNET Boot ROM required for ARCNET Boot)
No
1
A
A
Hard Disk Drive Present ?
Yes
Attempt to read boot sector
An error ?
Yes
No
<F1> or <1> pressed ?
Yes
Display Hard Disk Error Message
Stop
No
2
Floppy Disk Drive Present ?
Yes
Attempt to read boot sector
An error ?
Yes
No
No
B
C

B
C
D
E
3
F
G
<F2> or <2> pressed ?
Yes
Display Floppy Disk Error Message
No
Stop
<N> pressed ?
No
Sector 256 bytes, and no ref.s Model III ROM ?
Note: 1
Yes
Yes
Set Transfer Address to 43ØØH Note: 2
Model III ROM Image Present ? Note: 3
Yes
<L> pressed ?
No
Yes
No
Set Transfer Address to 3Ø15H Note: 2
Attempt to locate ROM Image on Floppy Disk Note: 4
ROM Image Found ? Note: 4
No
Yes
Write-enable Ø-37FFH (Mode 1)
Load ROM Image Note: 5
Errors while loading ROM Image ?
Yes
Set Transfer Address at end of ROM Image (Normally 3Ø15H) Note: 2
Display Error Message
Stop

G
ROM Image Present ?
No
Yes
<P> pressed ?
Yes
Display "ROM Image is loaded" message
Wait for <ENTER> or <BREAK> to be pressed
Write-protect memory (Mode Ø)
Set CPU speed to 2MHz
H

H
Switch boot ROM out of Memory
Jump to Transfer Address
7
Initialize RS-232 Port
Note: 6
Wait for Carrier Detect
Determine Correct Baud Rate
Transmit Baud Rate Detect Message
I

Notes:

(1) If the boot sector was not 256 bytes in length, then it is assumed to be a Model III package, and the ROM-image will be needed. If the sector is 256 bytes in length, then the sector is scanned for the sequence CDxx00H. The CD is the first byte of a Z80 unconditional subroutine call. The next byte can have any value. The third byte is tested against a zero. What this check does is test for any references to the first 256 bytes of memory. All Radio Shack Model III operating systems, and many other packages all reference the ROM at some point during the boot sector. Most boot sectors will display a message if the system cannot be loaded. To save space, these routines use the Model III ROM calls to display the message. Several ROM calls have their entry points in the first 256 bytes of memory, and these references are detected by the boot ROM.

Packages that do not reference the Model III ROM in the boot sector can still cause the Model III ROM image to be loaded by coding a CDxx00 somewhere in the boot sector. It does not have to be executable. At the same time, Model 4 packages must take care that there is no sequence of bytes in the boot sector that could be mis-interpreted to be a reference to the Boot ROM. An example of this would be sequence 06CD0E00, which is a LD B,0CDH and a LD C,0. If the boot sector cannot be changed, then the user must press the <F3> key each time the system is started to inform the ROM that the disk contains a Model III package which needs the Model III ROM-image.

(2) If you are loading a Model 4 operating system, then the boot ROM will always transfer control to the first byte of the boot sector, which is at 4300H. If you are loading a Model III operating system or about to use Model III ROM BASIC, then the transfer address is 3015H. This is the address of a jump vector in the "C" ROM of the Model III ROM image, and this will cause the system to behave exactly like a Model III. If the ROM-image file that is loaded has a different transfer address, then that address will be used when loading is complete. If the image is already present, it will use 3015H.

(3) Two different tests are done to insure that the Model III ROM image is present. The first test is to check ever third location starting at 3000H for a C3H. This is done for 10 locations. If any of these locations does not contain a C3H, then the ROM image is considered to be "not present". The next test is to check two bytes at location 000BH. If these addresses contain E9E1H, then the ROM image is considered to be "present".

(4) See Disk Director Searcher for more information.

(5) See File Loader for more information.

(6) The RS-232 loader is described under RS-232 Boot.

Disk Directory Searcher

When the Model III ROM image is to be loaded, it is always read from the floppy in drive 0.

Before the operation begins, some checks are made. First, the boot sector is read in from the floppy and the first byte is checked to make sure it is either a 00H or a FEH. If the byte contains some other value, no attempt will be made to read the ROM image from that disk. The location of the directory cylinder is then taken from the boot sector and the type of disk is determined. This is done by examining the Data Address Mark that

was picked up by the Floppy Disk Controller (FDC) during the read of the sector. If the DAM equals 1, the disk is a TRSDOS 1.x style disk. If the DAM equals 0, then the disk is a LDOS 5.1/ TRSDOS 6 style disk. This is important since TRSDOS 1.x disks number sectors starting with 1 and LDOS style disks number sectors starting with 0.

Once the disk type has been determined, an extra test is made if the disk is a LDOS style disk. This test reads the Granule Allocation Table (GAT) to determine if the disk is single sided or double sided.

The directory is then read one record at a time and a compare is made against the pattern 'MODEL% ' for the filename and 'III' for the extension. The '%' means that any character will match this position. If the user pressed one of the selection keys (A-G) during the keyboard scan, then that character is substituted in place of the '%' character. For example, if you pressed 'D', then the search would be for the file 'MODELD ', with the extension 'III'. The searching algorithm searches until it finds the entry or it reaches the end of the directory.

Once the entry has been found, the extent information for that file is copied into a control block for later use.

File Loader

The file loader is actually two modules — the actual loader and a set of routines to fetch bytes from the file on disk. The loader is invoked via a RST 28H. The byte fetcher is called by the loader using RST 20H. Since restart vectors can be re-directed, the same loader is used by the RS-232 boot. The difference is that the RST 20H is redirected to point to the RS-232 data receiving routine. The loader reads standard loader records and acts upon two types:

01 Data Load
1 byte with length of block, including address
1 word with address to load the data
n bytes of data, where n + 2 equals the length specified

02 Transfer Address
1 byte with the value of 02
1 word with the address to start execution at.

Any other loader code is treated as a comment block and is ignored. Once an 02 record has been found, the loader stops reading, even if there is additional data, so be sure to place the 02 record at the end of the file.

Floppy and Hard Disk Driver

The disk drivers are entered via RST 8H and will read a sector anywhere on a floppy disk and anywhere on head 1 (top-head) in a hard disk drive. Either 256 or 512 byte sectors are readable by these routines and they make the determination of the sector size. The hard disk driver is compatible with both the WD1000 and the WD1010 controllers. The floppy disk driver is written for the WD1793 controller.

Serial Loader

Invoking the serial loader is similar to forcing a boot from hard disk or floppy. In this case the right shift key must be pressed at some time during the first three seconds after reset. The program does not care if the key is pressed forever, making it convenient to connect pins 8 and 10 of the keyboard connector with a shorting plug for bench testing of boards. This assumes that the object program being loaded does not care about the key closure.

Upon entry, the program first asserts DTR (J4 pin 20) and RTS (J4 pin 4) true. Next, "Not Ready" is printed on the topmost line of the video display. Modem status line CD (J4 pin 8) is then sampled. The program loops until it finds CD asserted true. At that time the message "Ready" is displayed. Then the program sets about determining the baud rate from the host computer.

To determine the baud rate, the program compares data received by the UART to a test byte equal to '55' hex. The receiver is first set to 19200 baud. If ten bytes are received which are not equal to the test byte, the baud rate is reduced. This sequence is repeated until a valid test byte is received. If ten failures occur at 50 baud, the entire process begins again at 19200 baud. If a valid test byte is received, the program waits for ten more to arrive before concluding that it has determined the correct baud rate. If at this time an improper byte is received or a receiver error (overrun, framing, or parity) is intercepted, the task begins again at 19200 baud.

In order to get to this point, the host or the modem must assert CD true. The host must transmit a sequence of test bytes equal to '55' hex with 8 data bits, odd parity, and 1 or 2 stop bits. The test bytes should be separated by approximately 0.1 second to avoid overrun errors.

When the program has determined the baud rate, the message:

"Found Baud Rate x"

is displayed on the screen, where "x" is a letter from A to P, meaning:

A = 50 baud	E = 150	I = 1800	M = 4800
B = 75	F = 300	J = 2000	N = 7200
C = 110	G = 600	K = 2400	O = 9600
D = 134.5	H = 1200	L = 3600	P = 19200

The same message less the character signifying the baud rate is transmitted to the host, with the same baud rate and protocol. This message is the signal to the host to stop transmitting test bytes.

After the program has transmitted the baud rate message, it reads from the UART data register in order to clear any overrun error that may have occurred due to the test bytes coming in during the transmission of the message. This is because the receiver must be made ready to receive a sync byte signalling the beginning of the command file. For this reason, it is important that the host wait until the entire baud rate message (16 characters) is received before transmitting the sync byte, which is equal to 'FF' hex.

When the loader receives the sync byte, the message:

"Loading"

is displayed on the screen. Again, the same message is transmitted to the host, and, again, the host must wait for the entire transmission before starting into the command file.

If the receiver should intercept a receive error while waiting for the sync byte, the entire operation up to this point is aborted. The video display is cleared and the message:

"Error, x"

is displayed near the bottom of the screen, where "x" is a letter from B to H, meaning:

B = parity error
C = framing error
D = parity & framing errors
E = overrun error
F = parity & overrun errors
G = framing & overrun errors
H = parity & framing & overrun errors

The message:

"Error"

is then transmitted to the host. The entire process is then repeated from the "Not Ready" message. A six second delay is inserted before reinitialization. This is longer than the time required to transmit five bytes at 50 baud, so there is no need to be extra careful here.

If the sync byte is received without error, then the "Loading" message is transmitted and the program is ready to receive the command file. After receiving the "Loading" message the host can transmit the file without nulls or delays between bytes.

(Since the file represents Z80 machine code and all 256 combinations are meaningful, it would be disastrous to transmit nulls or other ASCII control codes as fillers, acknowledgement, or start-stop bytes. The only control codes needed are the standard command file control bytes.)

Data can be transmitted to the loader at 19200 baud with no delays inserted. Two stop bits are recommended at high baud rates.

See the File Loader description for more information on file loading.

If a receive error should occur during file loading, the abort procedure described above will take place, so when attempting remote control, it is wise to monitor the host receiver during transmission of the file. When the host is near the object board, as is the case in the factory application, or when more than one board is being loaded, it may be advantageous or even necessary to ignore the transmitted responses of the object board(s) and to manually pace the test byte, sync byte, and command file phases of the transmission process, using the video display for handshaking.

System Programmers Information

The Model 4P Boot ROM uses two areas of RAM while it is running. These are 4000H to 40FFH and 4300H to 43FFH. (For 512 byte boot sectors, the second area is 4300H to 44FFH.) If the Model III ROM Image is loaded, additional areas are used. See the technical reference manual for the system you are using for a list of these areas.

Operating systems that want to support a software restart by re-executing the contents of the boot ROM can accomplish this in one of two ways. If the operating system relies on the Model III ROM-Image, then jump to location 0 as you have in the past. If the operating system is a Model 4 mode package, a simple way is to code the following instructions in your assembly and load them before you want to reset:

Absolute Location	Instruction	
0000	DI	
0001	LD	A,1
0003	OUT	(9CH),A

These instructions cause the boot ROM to become addressable. After executing the OUT instruction, the next instruction executed will be one in the boot ROM. (These instructions also exist in the Model III ROM image at location 0.) The boot ROM has been written so that the first instruction is at address 0005. The hardware must be in memory mode 0 or else the boot ROM will not be switched in. This operation can be done with an OUT instruction and then a RST 0 can be executed to have the ROM switched in.

Restarts can be redirected at any time while the ROM is switched in. All restarts jump to fixed locations in RAM and these areas may be changed to point to the routine that is to be executed.

Restart	RAM Location	Default Use
0	none	Cold Start/Boot
8	4000H	Disk I/O Request
10	4003H	Display string
18	4006H	Display block
20	4009H	Byte Fetch (Called by Loader)
28	400CH	File Loader
30	400FH	Keyboard scanner
38	4012H	Reserved for future use
66	4015H	NMI (Floppy I/O Command Complete)

The above routines have fixed entry parameters. These are described here.

Disk I/O Request (RST 8H)

Accepts

A	1 for floppy, 2 for hard disk
B	Command Initialize 1 Restore 4 Seek 6 Read 12 (All reads have an implied seek)
C	Sector number to read The contents of the location disktype (405CH) are added to this value before an actual read. If the disk is a two sided floppy, just add 18 to the sector number.
DE	Cylinder number. (Only E is used in floppy operations)
HL	Address where data from a read operation is to be stored.

Returns

Z	Success, Operation Completed
NZ	Error, Error code in A

Error Codes

3	Hard Disk drive is not ready
4	Floppy disk drive is not ready
5	Hard Disk drive is not available
6	Floppy disk drive is not available
7	Drive Not Ready and no Index (Disk in drive, door open)
8	CRC Error
9	Seek Error
11	Lost Data
12	ID Not Found

Display String (RST 10H)

Accepts

HL	Pointer to text to be displayed. Text must be terminated with a null (0).
DE	Offset position on screen where text is to be displayed. (A 0000H will be the upper left-hand corner of the display.)

Returns

Success Always

A	Altered
DE	Points to next position on video
HL	Points to the null (0).

Display Block (RST 18H)

Accepts

HL	Points to control vector in the format:		
	+0	Screen Offset	
	+2	Pointer to text, terminated with null	
	+4	Pointer to text, terminated with null	
	..		
	+n	word FFFFH	End of control vector
or	+n	word FFFEH	Next word is new Screen Offset

If Z flag is set on entry, then the first screen offset is read from DE instead of from the control vector.

Each string is positioned after the previous string, unless a FFFEH entry is found. This is used heavily in the ROM to reduce duplication of words in error messages.

Returns

Success Always

DE	Points to next position on video

Byte Fetch (RST 20H)

Accepts None

Returns

Z	Success, byte in A
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call and:
2	ROM Image can't be loaded — Too many extents
10	ROM Image can't be loaded — Disk drive is not ready

File Loader (RST 28H)

Accepts None

Returns

Z	Success
NZ	Failure, error code in A

Errors

	Any errors from the disk I/O call of the byte fetch call and:
0	The ROM image was not found on drive 0

There are several pieces of information left in memory by the boot ROM which are useful to system programmers. These are shown below:

RAM Location	Description	
401DH	ROM Image Selected (% for none selected or A-G)	
4055H	Boot type	
	1 = Floppy	
	2 = Hard disk	
	3 = ARCNET	
	4 = RS-232C	
	5 - 7 = Reserved	
4056H	Boot Sector Size (1 for 256, 2 for 512)	
4057H	RS-232 Baud Rate (only valid on RS-232 boot)	
4059H	Function Key Selected	
	0 = No function key selected	
	<F1> or <1>	86
	<F2> or <2>	87
	<F3> or <3>	88
	<Caps>	85
	<Ctrl>	84
	<Left-Shift>	82
	<Right-Shift>	83
	Reserved	80-81 and 89-90
405BH	Break Key Indication (non-zero if <Break> pressed)	
405CH	Disk type	(0 for LDOS/ TRSDOS 6,1 for TRSDOS 1.x)

Keep in mind that Model III ROM image will initialize these areas, so this information is useful only to the Model 4 mode programmer.

5.2.7 RAM

Two configurations of Random Access Memory (RAM) are available on the Model 4P: 64K and 128K. The 64K and 128K option use the 6665-type 64K x 1 200NS Dynamic RAM, which requires only a single +5v supply voltage.

The DRAMs require multiplexed incoming address lines. This is accomplished by ICs U110 and U111 which are 74LS157 multiplexers. Data to and from the DRAMs are buffered by a 74LS245 (U118) which is controlled by Gate Array 4.2 (U106). The proper timing signals RAS0*, RAS1*, MUX*, and CAS* are generated by a delay line circuit U94. U116 (1/2 of a 74S112) and U117 (1/4 of a 74F08) are used to generate a precharge circuit. During M1 cycles of the Z80A in 4 MHz mode, the high time in MREQ has a minimum time of 110 nanosecs. The specification of 6665 DRAM requires a minimum of 120 nanosecs so this circuit will shorten the MREQ signal during the M1 cycle. The resulting signal PMREQ is used to start a RAM memory cycle through U114 (a 74S64). Each different cycle is controlled at U114 to maintain a fast M1 cycle so no wait states are required. The output of U114 (PRAS*) is ANDed with RFSH to not allow MUX* and CAS* to be generated during a REFRESH cycle. PRAS* also generates either RAS0* or RAS1*, depending on which bank of RAM the CPU is selecting. GCAS* generated by the delay line U94 is latched by U116 (1/2 of a 74S112) and held to the end of the memory cycle. The output of U116 is ANDed with VIDEO signal to disable the CAS* signal from occurring if the cycle is a video memory access. Refer to M1 Cycle Timing (Figure 5-8. and 5-9.), Memory Read and Memory Write Cycle Timing (Figure 5-10.) and (Figure 5-11.).

	STATE	LEVEL
SELØ =	Ø	ØV
SEL1 =	Ø	ØV
ROM =	1	ØV

	STATE	LEVEL
SELØ =	Ø	ØV
SEL1 =	Ø	ØV
ROM =	Ø	5V

Figure 5-22. Memory

	STATE	LEVEL
SELØ =	1	5V
SEL1 =	Ø	ØV
ROM =	Ø	5V

	STATE	LEVEL
SELØ =	1	5V
SEL1 =	Ø	ØV
ROM =	1	ØV

Figure 5-23. Memory

	STATE	LEVEL
SELØ =	Ø	ØV
SEL1 =	1	5V
ROM =	X	

	STATE	LEVEL
SELØ =	1	5V
SEL1 =	1	5V
ROM =	X	

Figure 5-24. Memory

Figure 5-25. M1 Cycle Timing (2MHZ)

Figure 5-26. M1 Cycle Timing (4MHZ)

Figure 5-27. Memory Read Cycle Timing

Figure 5-28. Memory Write Cycle Timing

Memory Map — Model 4P

Mode 0

SEL0 = 0 = 0V
SEL1 = 0 = 0V
ROM = 1 = 0V

0000 — 0FFF	Boot ROM	4K
1000 — 37FF	RAM (Read Only)	10K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 0

SEL0 = 0 = 0V
SEL1 = 0 = 0V
ROM = 0 = +5V

0000 — 37FF	RAM (Read Only)	14K
37E8 — 37E9	Printer Status (Read Only)	2
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1

SEL0 = 1 = +5V
SEL1 = 0 = 0V
ROM = 1 = 0V

0000 — 0FFF	Boot ROM	4K
0000 — 0FFF	RAM (Write Only)	4K
1000 — 37FF	RAM	10K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 1

SEL0 = 1 = +5V
SEL1 = 0 = 0V
ROM = 0 = +5V

0000 — 37FF	RAM	14K
3800 — 3BFF	Keyboard	1K
3C00 — 3FFF	Video	1K
4000 — FFFF	RAM	48K

Mode 2

SEL0 = 0 = 0V
SEL1 = 1 = +5V
ROM = X = Don't Care

0000 — F3FF	RAM	61K
F400 — F7FF	Keyboard	1K
F800 — FFFF	Video	2K

Mode 3

SEL0 = 1 = +5V
SEL1 = 1 = +5V
ROM = X = Don't Care

0000 — FFFF	RAM	64K

I/O Port Assignment

Port #	Normally Used	Out	In
FC — FF	FF	CASSOUT *	MODIN *
F8 — FB	F8	LPOUT *	LPIN *
F4 — F7	F4	DRVSEL *	(RESERVED)
F0 — F3	–	DISKOUT *	DISKIN *
F0	F0	FDC COMMAND REG.	FDC STATUS REG.
F1	F1	FDC TRACK REG.	FDC TRACK REG.
F2	F2	FDC SECTOR REG.	FDC SECTOR REG.
F3	F3	FDC DATA REG.	FDC DATA REG.
EC — EF	EC	MODOUT *	RTCIN *
E8 — EB	–	RS232OUT *	RS232IN *
E8	E8	UART MASTER RESET	MODEM STATUS
E9	E9	BAUD RATE GEN. REG.	(RESERVED)
EA	EA	UART CONTROL AND MODEM CONTROL REG.	UART STATUS REG.
EB	EB	UART TRANSMIT HOLDING REG.	UART HOLDING REG. (RESET D.R.)
E4 — E7	E4	WR NMI MASK REG. *	RD NMI STATUS *
E0 — E3	E0	WR INT MASK REG. *	RD INT MASK REG. *
A0 — DF	–	(RESERVED)	(RESERVED)
9C — 9F	9C	BOOT *	(RESERVED)
94 — 9B	–	(RESERVED)	(RESERVED)
90 — 93	90	SEN *	(RESERVED)
8C — 8F	–	GSEL0 *	GSEL0 *
88 — 8B	–	CRTCCS *	(RESERVED)
88, 8A	88	CRCT ADD. REG.	(RESERVED)
89, 8B	89	CRCT DATA REG.	(RESERVED)
84 — 87	84	OPREG *	(RESERVED)
80 — 83	–	GSEL1 *	GSEL1 *

I/O Port Description

Name: CASSOUT *
Port Address: FC — FF
Access: WRITE ONLY
Description: Output data to cassette or for sound generation

Note: The Model 4P **does not** support cassette storage, this port is only used to generate sound that was to be output via cassette port. The Model 4P sends data to onboard sound circuit.

D0 = Cassette output level (sound data output)

D1 = Reserved

D2 — D7 = Undefined

Name: MODIN * (CASSIN *)
Port Address: FC — FF
Access: READ ONLY
Description: Configuration Status

D0 = 0

D1 = CASSMOTORON STATUS

D2 = MODSEL STATUS

D3 = ENALTSET STATUS

D4 = ENEXTIO STATUS

D5 = (NOT USED)

D6 = FAST STATUS

D7 = 0

Name: LPOUT *
Port Address: F8 — FB
Access: WRITE ONLY
Description: Output data to line printer

D0 — D7 = ASCII BYTE TO BE PRINTED

Name: LPIN *
Port Address: F8 — FB
Access: READ ONLY
Description: Input line printer status

D0 — D3 = (RESERVED)

D4 = FAULT
1 = TRUE
0 = FALSE

D5 = UNIT SELECT
1 = TRUE
0 = FALSE

D6 = OUTPAPER
1 = TRUE
0 = FALSE

D7 = BUSY
1 = TRUE
0 = FALSE

Name: DRVSEL *
Port Address: F4 — F7
Access: WRITE ONLY
Description: Output FDC Configuration

Note: Output to this port will **ALWAYS** cause a 1-2 mscc. (Microsecond) wait to the Z80.

D0 = DRIVE SELECT 0

D1 = DRIVE SELECT 1

D2 = (RESERVED)

D3 = (RESERVED)

D4 = SDSEL
0 = SIDE 0
1 = SIDE 1

D5 = PRECOMPEN
0 = No write precompensation
1 = Write Precompensation enabled

D6 = WSGEN
0 = No wait state generated
1 = wait state generated

Note: This wait state is to sync Z80 with FDC chip during FDC operation.

D7 = DDEN *
0 = Single Density enabled (FM)
1 = Double Density enabled (MFM)

Name: DISKOUT *
Port Address: F0 — F3
Access: WRITE ONLY
Description: Output to FDC Control Registers

Port F0 = FDC Command Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignments)

Name: DISKIN *
Port Address: F0 — F3
Access: READ ONLY
Description: Input FDC Control Registers

Port F0 = FDC Status Register

Port F1 = FDC Track Register

Port F2 = FDC Sector Register

Port F3 = FDC Data Register

(Refer to FDC Manual for Bit Assignment)

Name: MODOUT *
Port Address: EC — EF
Access: WRITE ONLY
Description: Output to Configuration Latch

D0 = (RESERVED)

D1 = CASSMOTORON (Sound enable)
0 = Cassette Motor Off (Sound enabled)
1 = Cassette Motor On (Sound disabled)

D2 = MODSEL
0 = 64 or 80 character mode
1 = 32 or 40 character mode

D3 = ENALTSET
0 = Alternate character set disabled
1 = Alternate character set enabled

D4 = ENEXTIO
0 = External IO Bus disabled
1 = External IO Bus enabled

D5 = (RESERVED)

D6 = FAST
0 = 2 MHZ Mode
1 = 4 MHZ Mode

D7 = (RESERVED)

Name: RTCIN *
Port Address: EC — EF
Access: READ ONLY
Description: Clear Real Time Clock Interrupt

D0 — D7 = DON'T CARE

Name: RS232OUT *
Port Address: E8 — EB
Access: WRITE ONLY
Description: UART Control, Data Control, Modem Control, BRG Control

Port E8 = UART Master Reset

Port E9 = BAUD Rate Gen. Register

Port EA = UART Control Register (Modem Control Reg.)

Port EB = UART Transmit Holding Reg.

(Refer to Model III or 4 Manual for Bit Assignments)

Name: RS232IN *
Port Address: E8 — EB
Access: READ ONLY
Description: Input UART and Modem Status

Port E8 = MODEM STATUS

Port E9 = (RESERVED)

Port EA = UART Status Register

Port EB = UART Receive Holding Register (Resets DR)

(Refer to Model III or 4 Manual for Bit Assignments)

Name: WRNMIMASKREG *
Port Address: E4 — E7
Access: WRITE ONLY
Description: Output NMI Latch

D0 — D5 = (RESERVED)

D6 = ENMOTOROFFINT
0 = Disables Motoroff NMI
1 = Enables Motoroff NMI

D7 = ENINTRQ
0 = Disables INTRQ NMI
1 = Enables INTRQ NMI

Name: RDNMISTATUS *
Port Address: E4 — E7
Access: READ ONLY
Description: Input NMI Status

D0 = 0

D2 — D4 = (RESERVED)

D5 = RESET (not needed)
0 = Reset Asserted (Problem)
1 = *Reset Negated*

D6 = MOTOROFF
0 = Motoroff Asserted
1 = Motoroff Negated

D7 = INTRQ
0 = INTRQ Asserted
1 = INTRQ Negated

Name: WRINTMASKREG *
Port Address: E0 — E3
Access: WRITE ONLY
Description: Output INT Latch

D0 — D1 = (RESERVED)

D2 = ENRTC
0 = Real time clock interrupt disabled
1 = Real time clock interrupt enabled

D3 = ENIOBUSINT
0 = External IO Bus interrupt disabled
1 = External IO Bus interrupt enabled

D4 = ENXMITINT
0 = RS232 Xmit Holding Reg. empty int. disabled
1 = RS232 Xmit Holding Reg. empty int. enabled

D5 = ENRECINT
0 = RS232 Rec. Data Reg. full int. disabled
1 = RS232 Rec. Data Reg. full int. enabled

D6 = ENERRORINT
0 = RS232 UART Error interrupts disabled
1 = RS232 UART Error interrupts enabled

D7 = (RESERVED)

Name: RDINTSTATUS *
Port Address: E0 — E3
Access: READ ONLY
Description: Input INT Status

D0 — D1 = (RESERVED)

D2 = RTC INT

D3 = IOBUS INT

D4 = RS232 XMIT INT

D5 = RS232 REC INT

D6 = RS232 UART ERROR INT

D7 = (RESERVED)

Name: BOOT *
Port Address: 9C — 9F
Access: WRITE ONLY
Description: Enable or Disable Boot ROM

D0 = *ROM* *
0 = Boot ROM Disabled
1 = Boot ROM Enabled

D1 — D7 = (RESERVED)

Name: SEN *
Port Address: 90 — 93
Access: WRITE ONLY
Description: Sound output

D0 = SOUND DATA

D1 — D7 = (RESERVED)

Name: OPREG *
Port Address: 84
Access: WRITE ONLY
Description: Output to operation reg.

D0 = SEL0

D1 = SEL1

SEL1	SEL0	MODE
0	0	0
0	1	1
1	0	2
1	1	3

D2 = 8064
0 = 64 character mode
1 = 80 character mode

D3 = INVERSE
0 = Inverse video disabled
1 = Inverse video enabled

D4 = SRCPAGE — Points to the page to be mapped as new page
0 = U64K, L32K Page
1 = U64K, U32K Page

D5 = ENPAGE — Enables mapping of new page
0 = Page mapping disabled
1 = Page mapping enabled

D6 = DESPAGE — Points to the page where new page is to be mapped;
0 = L64K, U32K Page
1 = L64K, L32K Page

D7 = PAGE
0 = Page 0 of Video Memory
1 = Page 1 of Video Memory

5.2.8 Video Circuit

The heart of the video display circuit in the Model 4P is the 68045 Cathode Ray Tube Controller (CRTC), U42. The CRTC is a preprogrammed video controller that provides two screen formats: 64 by 16 and 80 by 24. The format is controlled by pin 3 of the CRTC (8064*). The CRTC generates all of the necessary signals required for the video display. These signals are VSYNC (Vertical Sync), HSYNC (Horizontal Sync) for proper sync of the monitor, DISPEN (Display Enable) which indicates when video data should be output to the monitor, the refresh memory addresses (MA0-MA13) which addresses the video RAM, and the row addresses (RA0-RA4) which indicates which scan line row is being displayed. The CRTC also provides hardware scrolling by writing to the internal Memory Start Address Register by OUTing to Port 88H. The internal cursor control of the 68045 is not used in the Model 4P video circuit.

Since the 80 by 24 screen requires 1,920 screen memory locations, a 2K by 8 static RAM (U82) is used for the video RAM. Addressing to the video RAM (U82) is provided by the 68045 when refreshing the screen and by the CPU when updating of the data is performed. These two sets of address lines are multiplexed by three 74LS157s (U41, U61, and U81). The multiplexers are switched by CRTCLK which allows the CRTC to address the video RAM during the high state of CRTCLK and the CPU access during the low state. A10 from the CPU is controlled by PAGE* which allows two display pages in the 64 by 16 format. When updates to the video RAM are performed by the CPU, the CPU is held in a WAIT state until the CRTC is not addressing the video RAM. This operation allows reads and writes to video RAM without causing hashing on the screen. The circuit that performs this function is a 74LS244 buffer (U84), an 8 bit transparent latch, 74LS373 (U83) and a Delay line circuit shared with Dynamic RAM timing circuit consisting of a 74LS74 (U98), 74LS32 (U96), 74LS04 (U95), 74LS00 (U92), 74LS02 (U69), and Delay Line (U94). During a CPU Read Access to the Video RAM, the address is decoded by the GA 4.2 and asserts VIDEO* low. This is inverted by U95 (1/6 of 74LS04) which pulls one input of U92 (1/4 of 74LS00) and in turn asserts VWAIT * low to the CPU. RD is high at this time and is latched into U98 (1/2 of 74LS74) on the rising edge of XADR7*, inverse of CRTCLK.

When RD is latched by U98, the Q output goes low releasing WAIT* from the CPU. The same signal also is sent to the Delay Line (U94) through U117 (1/4 of 74F08). The Delay line delays the falling edge 240 ns for VLATCH* which latches the read data from the video RAM at U83. The data is latched so the CRTC can refresh the next address location and prevent any hashing. MRD* decoded by U106 and a memory read is ORed with VIDEO* which enables the data from U83 to the data bus. The CPU then reads the data and completes the cycle. A CPU write is slightly more complex in operation. As in the RD cycle, VIDEO* is asserted low which asserts VWAIT* low to the CPU. WR is high at this time which is NANDed with VIDEO and synced with CRTCLK to create VRAMDIS that disables the video RAM output. On the rising edge of XADR7*, WR is latched into U98 (1/2 of 74LS74) which releases VWAIT* and starts cycle through the Delay Line. After 30ns DLYVWR* (Delayed video write) is asserted low which also asserts VBUFEN* (Video Buffer Enable) low. VBUFEN* enabled data from the Data bus to the video RAM. Approximately 120ns later DLYVWR* is negated high which writes the data to the video RAM and negates VBUFEN* turning off buffer. The CPU then completes WR cycle to the video RAM. Refer to Video RAM CPU Access Timing Figure 5-12 for timing of above RD or WR cycles.

During screen refresh, CRTCLK is high allowing the CRTC to address Video RAM. The data out of the video RAM is latched by LOAD* into Gate Array 4.3 (U102). INVERSE* determines if character should be alpha-numeric only (INVERSE* high) or unchanged (INVERSE* low). A9 is decoded with ENALTSET (Enable Alternate Set) and 7, which controls the alternate set in the character generator ROM. See ENALTSET Control Table below.

ENALTSET	Q7	Q6	A9
0	0	0	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

FIGURE 5-29. Video RAM CPU Access Timing

RA0-RA3, row addresses from the CRTC are used to control which scan line is being displayed. The Model 4P has a 4-bit full adder 74LS283 (U101) to modify the Row address. During a character display DLYGRAPHIC* is high which applies a high to all 4 bits to be added to row address. This will result in subtracting one from Row address count and allow all characters to be displayed one scan line lower. The purpose is so inverse characters will appear within the inverse block. When a graphic block is displayed DLYGRAPHIC* is low which causes the row address to be unmodified. Moving jumper from E14-E15 to E15-E16 will disable this circuit.

DLYCHAR* and DLYGRAPHICS are inverse signals and control which data is to be loaded into the internal shift register of U102. When DLYCHAR* is low and DLYGRAPHIC* is high, the Character Generator ROM (U103) is enabled to output data. When DLYCHAR* is high and DLYGRAPHIC* is low the graphics characters are internally buffered to the shift register. The data is loaded into the internal shift register on the rising edge of SHIFT* when LOADS* is low. Serial video data is output U102.19. The video information is inverted by U142 and F83, is filtered by R14 (47 ohm resistor), and C227 (100 pf Cap) and output to video monitor. VSYNC and HSYNC are buffered by (1/2 of 74LS86) U143 and are also output to video monitor. Refer to Video Circuit Timing Figure 5-30 and Inverse Video Timing Figure 5-19 for timing relationships of Video Circuit.

5.2.9 Keyboard

The keyboard interface of the Model 4P consists of open collector drivers which drive an 8 by 8 key matrix keyboard and an inverting buffer which buffers the key or keys pressed on the data bus. The open collector drivers (U57 and U77 (7416) are driven by address lines A0-A7 which drive the column lines of the keyboard matrix. The ROW lines of the keyboard are pulled up by a 1.5 kohm resistor pack RP2. The ROW lines are buffered and inverted onto the data bus by U78 (74LS240) which is enabled when KEYBD* is a logic low. KEYBD* is a memory mapped decode of addresses 3800-3BFF in Model III Mode and F400-F7FF in Model 4/4P mode. Refer to the Memory Map under Address Decode for more information. During real time operation, the CPU will scan the keyboard periodically to check if any keys are pressed. If no key is pressed, the resistor pack RP2 keeps the inputs of U78 at a logic high. U78 inverts the data to a logic low and buffers it to the data bus which is read by the CPU. If a key is pressed when the CPU scans the correct column line, the key pressed will pull the corresponding row to a logic low. U78 inverts the signal to a logic high which is read by the CPU.

5.2.10 Real Time Clock

The Real Time Clock circuit in the Model 4P provides a 30 Hz (in the 2 MHz CPU mode) or 60 Hz (in the 4 MHz CPU mode) interrupt to the CPU. By counting the number of interrupts that have occurred, the CPU can keep track of the time. The 60 Hz vertical sync signal (VSYNC) from the video circuitry is used for the Real Time Clock's reference. In the 2 MHz mode, FAST is a logic low which sets the Preset input, pin 4 of U23 (74LS74), to a logic high. This allows the 60 Hz (VSYNC) to be divided by 2 to 30 Hz. The output of 1/2 of U23 is ORed with the original 60 Hz and then clocks another 74LS74 (1/2 of U23). If the real time clock is enabled (ENRTC at a logic high), the interrupt is latched and pulls the INT* line low to the CPU. When the CPU recognizes the interrupt, the pulse is counted and the latch reset by pulling RTCIN* low. In the 4 MHz mode, FAST is a logic high which keeps the first half of U23 in a preset state (the Q* output at a logic low). The 60 Hz is used to clock the interrupts.

NOTE: If interrupts are disabled, the accuracy of the real time clock will suffer.

5.2.11 Line Printer Port

The Line Printer Port Interface consists of a pulse generator, an eight-bit latch, and a status line buffer. The status of the line printer is read by the CPU by enabling buffer U3 (74LS244). This buffer is enabled by LPRD* which is a memory map and port map decode. In Model III mode, only the status can be read from memory location 37E8 or 37E9. The status can be read in all modes by an input from ports F8-FB. For a listing of the bit status, refer to Port Map section.

After the printer driver software determines that the printer is ready for printing (by reading the correct status), the characters to be printed are output to Port F8-FB. U2, a 74LS374 eight-bit latch, latches the character byte and outputs to the line printer. One-half of U1 (74LS123), a one-shot, is then triggered which generates an appropriate strobe signal to the printer which signifies a valid character is ready. The output of the one-shot is buffered by 1/6th of the U51 (74LS04) to prevent noise from the printer cable from false-triggering the one-shot.

Figure 5-30. Video Circuit Timing

Figure 5-31. Video Blanking Timing

Figure 5-32. Inverse Video Timing

5.2.12 Graphics Port

The Graphics Port (J7) on the Model 4P is provided to attach the optional Graphics Board. The port provides D0-D7 (Data Lines), A0-A3 (Address Lines), IN*, GEN* and RESET* for the necessary interface signals for the Graphics Board. GEN* is generated by negative ORing Port selects GSEL0* (8C-8FH) and GSELI* (80-83H) together by (1/4 of 74LS08) U4. The resulting signal is negative ANDed with IORQ* by (1/4 of 74S32) U24. Seven timing signals are provided to allow synchronization of Main Logic Board Video and Graphics Board Video. These timing signals are VSYNC, HSYNC, DISPEN, DCLK, H, I, and J. Three control signals from the Graphics Board are used to sync to CPU access and select different video modes. WAIT* controls the CPU access by causing the CPU to WAIT till video is in retrace area before allowing any writes or reads to Graphics Board RAM. ENGRAF is asserted when Graphics video is displayed. ENGRAF also disables inverse video mode on Main Logic Board Video. CL166* (Clear 74L166) is used to enable or disable mixing of Main Logic Board Video and Graphics Board Video. If CL166* is negated high, then mixing is allowed in all for video modes 80 x 24, 40 x 24, 64 x 16, and 32 x 16. If CL166* is asserted low, this will clear the video shift register U63, which allows no video from the Main Logic Board. In this state 8064* is automatically asserted low to put screen in 80 x 24 video mode. Refer to Figure 5-16. Graphic Board Video Timing for timing relationships. Refer to the Model 4/4P Graphics Board Service information for service or technical information on the Graphics Board.

5.2.13 Sound

The sound circuit in the Model 4P is compatible with the Sound Board which was optional in the Model 4. Sound is generated by alternately setting and clearing data bit D0 during an OUT to port 90H. The state of D0 is latched by U129 (1/2 of a 74LS74) and the output is amplified by Q2 which drives a 8Ω speaker. The speed of the software loop determines the frequency, and thus, the pitch of the resulting tone. Since the Model 4P does not have a cassette circuit, some existing software that used the cassette output for sound would have been lost. The Model 4P routes the cassette latch to the sound board through U109. When the CASSMOTORON signal is a logic low, the cassette motor is off, then the cassette output is sent to the sound circuit.

5.2.14 I/O Bus Port

The Model 4P Bus is designed to allow easy and convenient interfacing of I/O devices to the Model 4P. The I/O Bus supports all the signals necessary to implement a device compatible with the Z80s I/O structure.

Addresses:

A0 to A7 allow selection of up to 256* input and 256 output devices if external I/O is enabled.

*Ports 80H to 0FFH are reserved for System use.

Data:

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus is external I/O is enabled.

Control Lines:

1. M1* — Z80A signal specifying an M1 or Operation Code Fetch Cycle or with IOREQ*, it specifies an Interrupt acknowledge.

2. IN* — Z80A signal specifying than an input is in progress. Logic AND of IOREQ* and WR*.

3. OUT* — Z80A signal specifying that an output is in progress. Logic AND of IOREQ* and WR*.

4. IOREQ* — Z80A signal specifying that an input or output is in progress or with M1*, it specifies an interrupt acknowledge.

5. RESET* — system reset signal.

6. IOBUSINT* — input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled.

7. IOBUSWAIT* — input to the CPU wait line allowing I/O Bus device to force wait states on the Z80 if external I/O is enabled.

8. EXTIOSEL* — input to I/O Bus Port circuit which switches the I/O Bus data bus transceiver and allows and INPUT instruction to read I/O Bus data.

The address line, data line, and all control lines except RESET* are enabled only when the ENEXIO bit in port EC is set to one.

To enable I/O interrupts, the ENIOBUSINT bit in the PORT E0 (output port) must be a one. However, even if it is disabled from generating interrupts, the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port).

See Model 4P Port Bit assignments for port 0FF, 0EC, and 0E0.

Figure 5-33. Graphic Board Video Timing

The Model 4P CPU board is fully protected from "foreign I/O devices" in that all the I/O Bus signals are buffered and can be disabled under software control. To attach and use and I/O device on the I/O Bus, certain requirements (both hardware and software) must be met.

For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software. This will enable the data bus address lines and control signals to the I/O Bus edge connector. When the input device is selected, the hardware should acknowledge by asserting EXTIOSEL* low. This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines. See Figure 5-17 for the timing. EXTIOSEL* can be generated by NANDing IN and the I/O port address.

Output port device use is the same as the input port device in use, in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software — in the same fashion.

For either input or output devices, the IOBUSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU. Note that since dynamic memories are used in the Model 4P, the wait line should be used with caution. Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time. It is recommended that the IOBUSWAIT* line be held active no more than 500 μsec with a 25% duty cycle.

The Model 4P will support Z80 Mode 1 interrupts. A RAM jump table is supported by the LEVEL II BASIC ROMs image and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F. When an interrupt occurs, the program will be vectored to the user-supplied address if I/O Bus interrupts have been enabled. To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H.

5.2.15 FDC Circuit

The TRS-80 Model 4P Floppy Disk Interface provices a standard 5-1/4" floppy disk controller. The Floppy Disk Interface supports both single and double density encoding schemes. Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one. The amount of write precompensation is 125 nsec and is not adjustable. One or two drives may be controlled by the interface. All data transfers are accomplished by CPU data requests. In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip. The end of the data transfer is indicated by generation of a non-maskable interrupt from the interrupt request output of the FDC chip. A hardware watchdog timer insures that any error condition will not hang the wait line to the CPU for a period long enough to destroy RAM contents.

Input or Output Cycles.

*Inserted by Z80 CPU

Input or Output Cycles with Wait States.

*Inserted by Z80 CPU

†Coincident with IORQ* only on INPUT cycle.

Figure 5-34. I/O Bus Timing Diagram

Control and Data Buffering

The Floppy Disk Controller Board is an I/O port-mapped device which utilizes ports E4H, F0H, F1H, F2H, F3H, and F4H. The decoding logic is implemented on the CPU board. (Refer to Paragraph 5.1.5 Address Decoding for more information on Port Map). U70 is a bi-directional, 8-bit transceiver used to buffer data to and from the FDC and RS-232 circuits. The direction of data transfer is controlled by the combination of control signals DISKIN*, RS232IN*, RDINT*, and RDNMI*. If any of these signals is active (logic low), U70 is enabled to drive data onto the CPU data bus. If both signals are inactive (logic high), U70 is enabled to receive data from the CPU board data bus. A second buffer (U36) is used to buffer the FDC chip data to the FDC/RS232 Data Bus, (BD0-BD7), U36 is enabled all the time and its direction controlled by DISKIN*. Again, if DISKIN* is active (logic low), data is enabled to drive from the FDC chip to the Main Data Busses. If DISKIN* is inactive (logic high), data is enabled to be transferred to the FDC chip.

Nonmaskable Interrupt Logic

Gate Array 4.4 (U18) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMI*. This enables the conditions which will generate a non-maskable interrupt to the CPU. The NMI interrupt conditions which are programmed by doing an OUT instruction to port E4H with the appropriate bits set. If data bit 7 is set, an FDC interrupt is enabled to generate an NMI interrupt. If data bit 7 is reset, interrupt requests request from the FDC are disabled. If data bit 6 is set, a Motor Time Out is enabled to generate an NMI interrupt. If data bit 6 is reset, interrupts on Motor Time Out are disabled. An IN instruction from port E4H enables the CPU to determine the source of the non-maskable interrupt. Data bit 7 indicates the status of FDC interrupt request (INTRQ) (0 = true, 1 = false). Data bit 6 indicates the status of Motor Time Out (0 = true, 1 = false). Data bit 5 indicates the status of the Reset signal (0 = true, 1 = false). The control signal RDNMI* gates this status onto the CPU data bus when active (logic low).

Drive Select Latch and Motor ON Logic

Selecting a drive prior to disk I/O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set. The following table describes the bit allocation of the Drive Select Latch:

Data Bit	Function
D0	Selects Drive 0 when set*
D1	Selects Drive 1 when set*
D2	Selects Drive 2 when set*
D3	Selects Drive 3 when set*
D4	Selects Side 0 when reset Selects Side 1 when set
D5	Write precompensation enabled when set, disabled when reset
D6	Generates WAIT if set
D7	Selects MFM mode if set Selects FM mode if reset

*Only one of these bits should be set per output

Hex D flip-flop U54 (74L174) latches the drive select bits, side select and FM*/MFM bits on the rising edge of the control signal DRVSEL*. Gate Array 4.4 (U18) is used to latch the Wait Enable and Write precompensation enable bits on the rising edge of DRVSEL*. The rising edge of DRVSEL* also triggers a one-shot (1/2 of U54, 74LS123) which produces a Motor On to the disk drives. The duration of the Motor On signal is approximately three seconds. The spindle motors are not designed for continuous operation. Therefore, the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected. The Motor On one-shot is retriggerable by simply executing another OUT instruction to the Drive Select Latch.

Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an OUT to the Drive Select Latch with D6 set. Pin 18 of U18 will go high after this operation. This signal is inverted by 1/4th of U15 and is routed to the CPU where it forces the Z80A into a wait state. The Z80A will remain in the wait state as long as WAIT* is low. Once initiated, the WAIT* will remain low until one of five conditions is satisfied. If INTRQ, DRQ, and RESET, inputs become active (logic high), it causes WAIT* to go high which allows the Z80 to exit the wait state. An internal timer in U18 serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents. This internal watchdog timer logic will limit the duration of a wait to 1024μsec, even if the FDC chip should fail to generate a DRQ or an INTRQ.

If an OUT to Drive Select Latch is initiated with D6 reset (logic low), a WAIT is still generated. The internal timer in U18 will count to 2 which will clear the WAIT state. This allows the WAIT to occur only during the OUT instruction to prevent violating any Dynamic RAM parameters.

NOTE: This automatic WAIT will cause a .5-1 μsec wait each time an out to Drive Select Latch is performed.

Clock Generation Logic

A 16 MHz crystal oscillator and a Gate Array 4.4 (U18) are used to generate the clock signals required by the FDC board. The 6 MHz oscillator is implemented internal to U18 and a quartz crystal (Y2). The output of the oscillator is divided by 2 to generate an 8 MHz clock. This is used by the FDC 1773 for all internal timing and data separation. U18 further divides the 16 MHz clock to drive the watchdog timer circuit.

Disk Bus Output Drivers

High current open collector drivers U15 and U34 are used to buffer the output signals from the FDC circuit to the disk drives.

Write Precompensation and Write Data Pulse Shaping Logic

All Write Precompensation is generated internal to the FDC chip 1773 (U17). Write Precompensation is enabled when W6 goes high and Write Precompensation is enabled from software. This signal is multiplexed with RDY by W6 is fed into pin 20 of U17. Write Data is output pin 22 of U17 and is shaped by a one-shot (1/2 of U56) which stretches the data pulses to approximately 500 nsec.

Floppy Disk Controller Chip

The 1773 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation. The following port addresses are assigned to the internal registers of the 1773 FDC chip:

Port No.	Function
F0H	Command/Status Register
F1H	Track Register
F2H	Sector Register
F3H	Data Register

5.2.16 RS-232-C Circuit

RS-232C Technical Description

The RS-232C circuit for the Model 4P computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input-output interface connector (J4). The heart of the circuit is the TR1865 Asynchronous Receiver/Transmitter U33. It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop, and parity bits. For a more detailed description of how this LSI circuit performs these functions, refer to the TR1865 data sheets and application notes. The transmit and receive clock rates that the TR1865 needs are supplied by the Baud Rate Generator U73 (BR1943). This circuit takes the 5.0688 MHz supplied by the system timing circuit and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks. The rates available from the BRG go from 50 Baud to 19200 Baud. See the BRG table for the complete list.

BRG Programming Table

Nibble Loaded	Transmit/ Receive Baud Rate	16X Clock	Supported by SETCOM
0H	50	0.8 kHz	Yes
1H	75	1.2 kHz	Yes
2H	110	1.76 kHz	Yes
3H	134.5	2.1523 kHz	Yes
4H	150	2.4 kHz	Yes
5H	300	4.8 kHz	Yes
6H	600	9.6 kHz	Yes
7H	1200	19.2 kHz	Yes
8H	1800	28.8 kHz	Yes
9H	2000	32.081 kHz	Yes
AH	2400	38.4 kHz	Yes
BH	3600	57.6 kHz	Yes
CH	4800	76.8 kHz	Yes
DH	7200	115.2 kHz	Yes
EH	9600	153.6 kHz	Yes
FH	19200	307.2 kHz	Yes

The RS-232C circuit is port mapped and the ports used are E8 to EB. Following is a description of each port on both input and output.

Port	Input	Output
E8	Modem status	Master Reset, enables UART control register load
EA	UART status	UART control register load and modem control
E9	Not Used	Baud rate register load enable bit
EB	Receiver Holding register	Transmitter Holding register

Interrupts are supported in the RS-232C circuit by the Interrupt mask register and the Status register internal to GA 4.5 (U31) which allow the CPU to see which kind of interrupt has occurred. Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors — parity, framing, or data overrun. This allows a minimum of CPU overhead in transferring data to or from the UART. The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read). Refer to the IO Port description for a full breakdown of all interrupts and their bit positions.

All Model I, III, and 4 software written for the RS-232-C interface is compatible with the Model 4P RS-232-C circuit, provided the software does not use the sense switches to configure the interface. The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface. The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145).

Pinout Listing

The following list is a pinout description of the DB-25 connector (P1).

Pin No.	Signal
1	PGND (Protective Ground)
2	TD (Transmit Data)
3	RD (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear To Send)
6	DSR (Data Set Ready)
7	SGND (Signal Ground)
8	CD (Carrier Detect)
19	SRTS (Spare Request to Send)
20	DTR (Data Terminal Ready)
22	RI (Ring Indicate)

5.2.17 CPU Board Troubleshooting Guide

This section is a general guide for service personnel to check out and troubleshoot the Model 4P Main Logic CPU Board. Procedures in section 4 Troubleshooting should be followed before proceeding to following steps. This guide will provide step by step procedures to help isolate the faulty area on the CPU board. Knowledge of each area of the CPU board is necessary to determine exact component failure. Refer of CPU Board Schematics and Theory of Operation during troubleshooting for specific check points and testing.

1. No video messages are displayed and correct data does not appear at video output connector J9.
   If above condition exists, go to 2; if video okay, but Model 4P does not boot properly, go to 10.
   If video and boot-up is okay, go to 15.

2. Check for video timing signal DCLK from Gate Array 4.1 (U148) in 64 x 16 and 80 x 24.
   If okay, go to 3; if one or both modes bad, go to 7.

3. Check for proper timing signals output from U148 (SHIFT*, XADR7*, CRTCLK, POT*, LOAD*, LOADS*).
   If okay, then go to 4; if one or more bad, replace U148 or U128.

4. Check if 68046 U42 is working properly and has correct input signals.
   If all okay, then go to 5. If bad, replace U42 or check for input signals where they originate.

5. Check for timing and proper signals U102.
   If bad, replace as necessary; if okay, go to 6.

6. Check output of pin 4 of U142 and repair as necessary.

7. Check for 20M clock at pin 2 of U148.
   If okay, go to 8; if bad, replace Y1 or U148.

8. Check for outputs of U148 (PCLK, RS232CLK).
   If okay, then go to 9; if any bad, replace U148.

9. Check for 12M at output of U146 pin 8.
   If okay, then video should work; if bad, replace 146.

10. Run Memory Test in Boot ROM by holding down period (.) and toggling Reset.
    If memory checks okay, then go to 11; if not, check memory circuit and/or replace RAM chips.

11. Check Clock circuit of Floppy Disk Controller.
    If 16MHz and 8 MHz okay, go to 12; if bad, repair or replace necessary components.

12. Check for all incoming signals to the FDC chip U17.
    If any bad, repair as necessary; if okay, go to 13.

13. Check all handshaking signals to FDC chip from CPU.
    If okay, go to 14; if bad, repair as necessary.

14. Check Data Bus and control lines.
    If okay, then problem still exists in Floppy Disk Circuit or Floppy Disk Drive. Refer to each section accordingly. If bad, replace as necessary.

15. If unit boots okay, then boot Model 4P Diagnostics Diskette and execute each diagnostic to isolate any minor problems on CPU Board.

ZONE	LTR	REVISION DESCRIPTION	DATE	APPROVED
		RELEASED FOR PRODUCTION	5/31/84	

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RELEASED FOR PRODUCTION

REF: DRILL PLAN #1700254, REV. A

	DATE	TITLE
DRAFT	4/23/84	SCHEMATIC– MAIN LOGIC MODEL 4P GATE ARRAY
CHECK	5/30/84	
DESIGN	5/30/84	
APPD	5/30/84	
APPD	5-31-84	

tandy

DWG NO	SIZE
8000233	D
SCALE N/A	SHEET 1 OF 7

NOTE (UNLESS OTHERWISE SPECIFIED):
1. ALL RESISTANCE VALUES ARE IN OHMS, K=1000.

CPU AND TIMING

0059,0067 544

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SELECT AND DECODE LOGIC

DRAWING NO.	REV
8000233	
SCALE N/A	SHEET 2 OF 7

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MEMORY CONTROL AND MEMORY

DRAWING NO.	REV
8000233	
SCALE N/A	SHEET 3 OF 7

DRAWING NO.	REV.
8000233	
SCALE N/A	SHEET 4 OF 7

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DRAWING NO.	REV
8000233	
SCALE N/A	SHEET 5 OF 7

PORT LOGIC

DRAWING NO.	REV.
8000233	
SCALE N/A	SHEET 6 OF 7

FLOPPY DISK CONTROLLER LOGIC

RS232C LOGIC

DRAWING NO.	REV.
8000233	
SCALE N/A	SHEET 7 OF 7

FRONT SILKSCREEN

TANDY CORP 8709524 REV —
FRONT
325.4
350.8
TANDY INC. 02-Mar-84 TANSRS
GESSL1 PAD=15E6-1 VIA=1

TANDY CORP
8709524 REV —
REAR
1983 MADE IN USA
TANDY CORP.
1700284
8709524
REV —
350.8
325.4
scale = 1.00
TAN5RS 02-Mar-84 TANDY INC.
VIA=1 SEG=0 PAD=0 GESSL0

Parts List

Model 4P Gate Array PC Board

Sym	Description	Part Number
C1-6	Capacitor .1 mfd 50V Mono Axial	8374104
C9-18	Capacitor .1 mfd 50V Mono Axial	8374104
C22-24	Capacitor .1 mfd 50V Mono Axial	8374104
C27-31	Capacitor .1 mfd 50V Mono Axial	8374104
C33	Capacitor .1 mfd 50V Mono Axial	8374104
C34	Capacitor .1 mfd 50V Mono Axial	8374104
C36	Capacitor .1 mfd 50V Mono Axial	8374104
C41	Capacitor .1 mfd 50V Mono Axial	8374104
C42	Capacitor .1 mfd 50V Mono Axial	8374104
C45	Capacitor .1 mfd 50V Mono Axial	8374104
C50	Capacitor .1 mfd 50V Mono Axial	8374104
C55-57	Capacitor .1 mfd 50V Mono Axial	8374104
C61	Capacitor .1 mfd 50V Mono Axial	8374104
C67	Capacitor .1 mfd 50V Mono Axial	8374104
C69	Capacitor .1 mfd 50V Mono Axial	8374104
C70	Capacitor .1 mfd 50V Mono Axial	8374104
C72	Capacitor .1 mfd 50V Mono Axial	8374104
C73	Capacitor .1 mfd 50V Mono Axial	8374104
C77	Capacitor .1 mfd 50V Mono Axial	8374104
C78	Capacitor .1 mfd 50V Mono Axial	8374104
C81-89	Capacitor .1 mfd 50V Mono Axial	8374104
C91	Capacitor .1 mfd 50V Mono Axial	8374104
C92	Capacitor .1 mfd 50V Mono Axial	8374104
C94-96	Capacitor .1 mfd 50V Mono Axial	8374104
C98	Capacitor .1 mfd 50V Mono Axial	8374104
C101-106	Capacitor .1 mfd 50V Mono Axial	8374104
C108-111	Capacitor .1 mfd 50V Mono Axial	8374104
C114-118	Capacitor .1 mfd 50V Mono Axial	8374104
C121	Capacitor .1 mfd 50V Mono Axial	8374104
C124	Capacitor .1 mfd 50V Mono Axial	8374104
C125	Capacitor .1 mfd 50V Mono Axial	8374104
C129	Capacitor .1 mfd 50V Mono Axial	8374104
C133-140	Capacitor .1 mfd 50V Mono Axial	8374104
C142	Capacitor .1 mfd 50V Mono Axial	8374104
C143	Capacitor .1 mfd 50V Mono Axial	8374104
C146	Capacitor .1 mfd 50V Mono Axial	8374104
C148	Capacitor .1 mfd 50V Mono Axial	8374104
C153-160	Capacitor .1 mfd 50V Mono Axial	8374104
C201-211	Capacitor 22 mfd 16V Elec. Rad	8326221
C212	Capacitor 1000 pfd 50V C. Disk Rad	8302104
C213	Capacitor .022 mfd 50V C. Disk	8303224
C214	Capacitor .022 mfd 50V C. Disk	8303224
C215	Capacitor 10 mfd 16V Elec. Rad	8326101
C216	Capacitor 33 pfd 50V C. Disk Npo Ax	8300334
C217,	Capacitor 22 pfd 50V C. Disk NPO Ax	8300224
C218	Capacitor .1 mfd 50V Mono Axial	8374104
C219	Capacitor 200 pfd 50V C. Disk Z5U Rad	8301223
C220	Capacitor 22 pfd 50V C. Disk NPO Ax	8300224

Parts List

Model 4P Gate Array PC Board

Sym	Description	Part Number
C221	Capacitor 22 pfd 50V C. Disk NPO Ax	8300224
C222	Capacitor 100 pfd 50V C. Disk Ax	8301104
C223	Capacitor 100 pfd 50V C. Disk Ax	8301104
C224	Capacitor .1 mfd 50V Mono Axial	8374104
C226	Capacitor 100 pfd 50V C. Disk Ax	8301104
C227	Capacitor 100 pfd 50V C. Disk Ax	8301104
C228	Capacitor .1 mfd 50V Mono Axial	8374104
CR1	Diode 1N4148	8150148
E1-8,14-16	Staking Pins	8529014
FB1-4	Ferrite Bead	8419014
J4	Connector, 25-Pin (RS232) DB25	8519109
J5	Connector, 34-Pin (Floppy Disk) Header	8519120
J6	Connector, Dual 8 (Keyboard) Header Rt. Angle	8519184
J7	Connector, 34-Pin (Graphics) Header	8519120
J8	Connector, 3-Pin (Reset) Header	8519215
J9	Connector, 6-Pin (Video) Header	8519211
J10	Connector, 4-Pin (Power) Header	8519210
Q1	Transistor 2N3906	8100906
R1	Resistor 20 kohm 1/4W 5%	8207320
R2	Resistor 160 kohm 1/4W 5%	8207416
R3-5	Resistor 4.7 kohm 1/4W 5%	8207247
R6	Resistor 4.7 Meg ohm 1/4W 5%	8207457
R8	Resistor 4.7 kohm 1/4W 5%	8207247
R9	Resistor 22 ohm 1/4W 5%	8207022
R10	Resistor 47 ohm 1/4W 5%	8207047
R11	Resistor 56 ohm 1/4W 5%	8207056
R12	Resistor 4.7 kohm 1/4W 5%	8207247
R13	Resistor 27 ohm 1/4W 5%	8207027
R14	Resistor 47 ohm 1/4W 5%	8207047
R15-17	Resistor 150 ohm 1/4W 5%	8207115
R18	Resistor 3.6 kohm 1/4W 5%	8207236
R19	Resistor 22 ohm 1/2W 5%	8217022
R20	Resistor 4.7 kohm 1/4W 5%	8207247
R21-23	Resistor 27 ohm 1/4W 5%	8207027
R24	Resistor 2.2 kohm 1/4W 5%	8207222
R25	Resistor 100 kohm 1/4W 5%	8207410
R26	Resistor 750 ohm 1/4W 5%	8207175
R27	Resistor 4.7 kohm 1/4W 5%	8207247
R28	Resistor 10 kohm 1/4W 5%	8207310
R29	Resistor 10 kohm 1/4W 5%	8207310
R30	Resistor 150 ohm 1/4W 5%	8207115

Parts List

Model 4P Gate Array PC Board

Sym	Description	Part Number
RP1	Resistor Pak 27 ohm DIP 16-Pin	8290027
RP2	Resistor Pak 1.5 kohm SIP 10-Pin	8290015
RP4	Resistor Pak 150 ohm SIP 10-Pin	8290013
S1	Speaker 8 ohm	8490008
U1	IC 74LS123 Multivibrator	8020123
U2	IC 74LS374 Flip Flop	8020374
U3	IC 74LS244 Octal Buffer	8020244
U4	IC 74LS08 Quad 2-In AND	8020008
U5	IC 74LS04 Hex Inverter	8020004
U6	IC 74LS245 Tranceiver	8020245
U9	IC 74LS244 Octal Buffer	8020244
U10	IC 74LS367 Hex Driver	8020367
U11	IC 1489 Receiver	8050189
U12	IC 1488 Driver	8050188
U13	IC 1489 Receiver	8050189
U14	IC 7416 Hex Inverter	8000016
U15	IC 7416 Hex Inverter	8000016
U16	IC 74LS367 Hex Driver	8020367
U17	IC WD1773	8040773
U18	IC 4.4 Floppy Support Array	8040544
U22	IC 74LS02 2-In NOR	8020002
U23	IC 74LS74 Flip Flop	8020074
U24	IC 74LS32 Quad 2-In OR	8020032
U27	IC 74LS244 Octal Buffer	8020244
U28-30	IC 74LS138 Quad 2-In NAND	8020138
U31	IC 4.5 RS232C Support Array	8040545
U33	IC TR1865 UART	8040865
U34	IC 74LS174 Hex Flip-Flop	8020174
U36	IC 74LS245 Tranceiver	8020245
U41	IC 74LS157 Multiplexer	8020157
U42	IC 68A045 CRTC	8040045
U45	IC Z80A CPU	8047880
U50	IC 74LS21 Dual 4-In AND	8020021
U55	IC 74LS08 Quad 2-In AND	8020008
U56	IC 74LS123 Multivibrator	8020123
U57	IC 7416 Hex Inverter	8000016
U61	IC 74LS157 Multiplexer	8020157
U67	IC 74LS244 Octal Buffer	8020244
U69	IC 68A332 4K X 8 300NS ROM	8075332
U70*	IC 74LS245 Tranceiver	8020245
U72	IC 74LS244 Octal Buffer	8020244
U73	IC BR1943 Clock Gen.	8040943
U77	IC 7416 Hex Inverter	8000016
U78	IC 74LS240 Octal Buffer	8020240

* NOTE: Starred (*) IC to be socketed

Parts List

Model 4P Gate Array PC Board

Sym	Description	Part Number
U81	IC 74LS157 Multiplexer	8020157
U82	IC 4016 2K X 8 RAM Static 200NS	8040116
U83	IC 74LS373 Octal Latch	8020373
U84	IC 74LS244 Octal Buffer	8020244
U85	IC 74LS273 Octal Flip-Flop	8020273
U86*	IC 74LS245 Tranceiver	8020245
U87	IC 74F04 Hex Inverter	8015004
U88	IC 74LS11 Triple 3-In AND	8020011
U89	IC 74LS27 Triple 3-In NOR	8020027
U91	IC 74LS04 Hex Inverter	8020004
U92	IC 74LS00 Quad 2-In NAND	8020000
U94	Delay Line	8429020
U95	IC 74LS04 Hex Inverter	8020004
U96	IC 74LS32 Quad 2-In OR	8020032
U98	IC 74LS74 Flip Flop	8020074
U101	IC 74LS283 Binary Adder	8020283
U102	IC 4.3 Video Support Array	8040543
U103	IC MCM68A316E Character ROM	8049007
U104	IC 74LS04 Hex Inverter	8020004
U105	IC 74LS32 Quad 2-In OR	8020032
U106	IC 4.2 Address Decode Array	8040542
U108	IC 74LS51 AND-OR Invert	8020051
U109	IC 74LS02 2-In NOR	8020002
U110	IC 74LS157 Multiplexer	8020157
U111	IC 74LS157 Multiplexer	8020157
U114	IC 74S64 AND-OR-Invert	8010064
U115	IC 74S32 Quad 2-In OR	8010032
U116	IC 74S112 J-K Flip Flop	8010112
U117	IC 74F08 Quad 2-In AND	8015008
U118	IC 74LS245 Tranceiver	8020245
U121	IC 74LS14 Hex Inverter	8020014
U124	IC 74LS174 Hex Flip-Flop	8020174
U125	IC 74LS244 Octal Buffer	8020244
U129	IC 74LS74 Flip Flop	8020074
U133-140	IC MCM6665 64K DRAM 200NS	8040665
U142	IC 74LS02 2-In NOR	8020002
U146	IC PLL Multimodule	8409036
U148	IC 4.1 System Timing Array	8040541

* NOTE: Starred (*) IC to be socketed

Parts List

Model 4P Gate Array PC Board

Sym	Description	Part Number
U17	Socket 28-Pin DIP	8509007
U18,	Socket 24-Pin DIP	8509001
U31	Socket 40-Pin DIP	8509002
U33	Socket 40-Pin DIP	8509002
U42	Socket 40-Pin DIP	8509002
U45	Socket 40-Pin DIP	8509002
U69,	Socket 24-Pin DIP	8509001
U70	Socket 20-Pin DIP	8509009
U73	Socket 18-Pin DIP	8509006
U82,	Socket 24-Pin DIP	8509001
U86	Socket 20-Pin DIP	8509009
U102	Socket 40-Pin DIP	8509002
U103	Socket 24-Pin DIP	8509001
U106	Socket 40-Pin DIP	8509002
U133-140,	Socket 16-Pin DIP	8509003
U148	Socket 24-Pin DIP	8509001
U153-160,	Socket 16-Pin DIP	8509003
Y1	Crystal 20.2752 MHz (2 Lead)	8409031
Y2	Crystal 16 MHz Parallel Resonant	8409038
	Low Cost Model 4P PC Board Sub Assy.	8858011
	Low Cost Model 4P Board Rev. "-"	8709524

5.3 MINI-DISK DRIVES

The Model 4P utilizes two 5-1/4" Flexible Disk Drive assemblies. These drives are internally mounted with Drive 0 at the left and Drive 1 at the right when facing the CRT display. They are compact, low profile drives that require only half the space normally required. The drives use an ANSI-compatible, Industry Standard, 5-1/4 inch diskette and contain 48 tracks per inch.

Two different types of drives are used in the Model 4P. One is a double-sided recording device. Both are capable of reading and writing in single-density format on a diskette. The drives have double density capability when a Modified Frequency Modulated (MFM) or other appropriate recording technique is used. Encoding and decoding of the data is done by the user's controller.

Service information and schematics for the Mini-Disk Drive are contained in the Manufacturer's Operating and Service Manual at the rear of this manual.

5.4 POWER SUPPLY ASSEMBLY

5.4.1 Power Supply

Basic Principle

A switching power supply circuit employs a high-speed semiconductor switch to control the storage and release of electrical energy in an inductor and provide regulated DC output voltages with a minimum loss of energy in heat-dissipating elements. There are several schemes for achieving this result which differ primarily in the arrangement of the basic circuit elements. These elements include a switch, an inductor, a rectifier, a capacitor and a DC voltage source.

An arrangement well-suited for economical power supplies with rated power outputs under 100 watts is the FLYBACK CONVERTER shown in Figure 5-35. The waveforms in Figure 5-36 are used to describe the operation of the Flyback Converter circuit. For the purpose of this discussion we will assume that the duration of the "ON" time equals the duration of the "OFF" time and Vo = rated output voltage.

Figure 5-35. Basic Flyback Converter

Figure 5-36.

When the switch is closed (ON) at time ta, Vin is impressed across the primary winding of inductor L and the current Isw increases linearly from zero until the switch opens (OFF) at time tb. Note that Isec is zero while the switch is closed. This is because Vsec is negative with respect to Vo thus reverse-biasing diode D. Note that Vsw is also zero while the switch is closed.

When the switch opens at time tb, the magnetic field of L instantly collapses and reverses polarity. At this moment, Vsw is equal to Vin plus the voltage across L just before the switch opened (also equal to Vin). Therefore, at the instant the magnetic field reverses polarity, Vsw = 2Vin.

During the interval when the switch is open (tb to tc), the secondary voltage, Vsec, is a replica of the primary voltage Vsw. Diode D is now forward biased due to the polarity of the inductor windings and because the turns ratio, n, is such that:

$$Vsec \times n > Vo$$

This biasing replenishes the charge in capacitor C that was delivered to the load R during the ta-tb interval. This is the "flyback" interval and is so named because the inductor releases the energy stored in its magnetic field while the switch is OFF.

Several other facts are illustrated by the waveforms of Figure 5-36. First, the voltage across the switch Vsw decays exponentially from 2Vin to Vin during the "OFF" interval. This is because the inductor and the switch timing are adjusted to transfer all of the energy that was stored in the inductor while the switch was ON, into the secondary while the switch is OFF. (Observe that Isec DECREASES linearly with time to zero at the end of the "OFF" time period.) This is known as resetting the core. Thus, at time tc when the switch is ready to turn on again, the DC input voltage Vin is again available to charge the inductor. Also at this time, all currents in the inductor are zero.

Second, since we have assumed that Isw increases linearly with time and that the ON and OFF time periods are equal (50% duty cycle), the average current in the primary, Isw (av), is 1/4 the peak current Isw. Also, the average current in the secondary, which is equal to the load current Io, is 1/4 the peak current in the secondary.

Third, the turns ratio is set by the ratio of the average primary voltage (Vsw) over a full cycle at its lowest value to the maximum permissible output voltage, Vo. The lowest Vsw value occurs at low AC line and maximum output load. In practice, the actual turns ratio, the ratio of peak-to-average voltages and currents, and the duty cycle may be adjusted to compensate for circuit losses.

Fourth, notice the ringing or oscillation that appears on the peak portion of Vsw and Vsec. This oscillation occurs at the resonant frequency of the leakage inductance of the inductor L and the parasitic capacitance of the circuit. The parasitic capacitance includes the interwinding capacitance of the inductor and stray capacitance of the switch. If this oscillatiion is not damped by a suitable means, the peak voltages may easily exceed the breakdown rating of the switch or the insulation in the inductor.

Block Diagram

The basic circuit illustrated in Figure 5-35 can be divided into three functional blocks: Input DC supply, primary, and secondary. To make use of this model, we need to expand it to provide control for the switch timing and to include sufficient circuitry to satisfy performance and reliability specifications. The complete block diagram is shown in Figure 5-37.

Figure 5-37. Power Supply Block Diagram

The other blocks provide additional output voltages, add safety or protective features, reduce circuit noise, and develop signals for use by the control section. The control section continuously operates the bipolar transistor switch and varies the proportion of ON time to OFF time in response to changes in AC input line voltage or output load current. This is accomplished by feeding back a signal from the output terminals and instructs the control section to increase or decrease the ON time to compensate for a change in the output voltage.

The DC voltage supply to the control section is controlled by the latch circuit when AC power is first applied to the power supply. A built-in timing circuit allows the input DC supply filter capacitor to become fully charged before power is applied to the control section. After the control section circuit starts and secondary voltages reach their regulated output levels, the auxiliary power supply provides the required DC voltage to operate the control section. The latch is reset when the current limit or under-voltage sensors operate, thus removing DC voltage to the Control IC.

There are four secondary or output voltages in addition to the auxiliary supply: +5.05 volt, +12 volt CRT, +12 volt Disk, and −12 volt. The +5.05 and +12 DISK voltages are regulated by the control circuit response to the frequency compensated feedback control signal which comes from the load sense section. Since the load sensing occurs on the secondary side, an optical coupler circuit is necessary to provide safety isolation between the primary side common ground and the secondary side common ground.

All secondary voltages, including the auxiliary +12 voltage, share the same magnetic flux linkage in the transformer core and are controlled by the flyback inductor. Any change in secondary load currents cause a change in the shared magnetic flux. This change in the flux of the inductor sets up an EMF (electromotive force) which causes a flux in opposition to the one which resulted from the change in load current. Thus, the original change tends to be counteracted and the current delivered to the load remains constant.

The output filters reduce the remaining ripple voltage components of the AC line and switching frequencies to levels low enough to prevent interference with the circuits operated by the supply. Switching frequency components that could be conducted out the AC input terminals are suppressed by the EMI filter to avoid interference with other equipment connected to the power line.

The overvoltage crowbar senses an abnormal rise in the +5.1 volt output and short-circuits the voltage line to the common secondary ground, thus tripping the current limiting circuit which finally shuts down the supply.

The surge limiter at the AC line input prevents the input filter capacitor in-rush current surge from exceeding component ratings or unnecessarily tripping external fuses.

5.4.2 Technical Specifications

Environment:

Temperature; Operating Storage	0 to 50 C (32 to 122 F)
	−40 to 85 C (−40 to 185 F)
Humidity; Operating Storage	85% r.h. @ 35 C (95 F) max.
	95% r.h. @ 55 C (131 F) max.

Input Voltage:
90 to 135 VAC rms, 47 to 63 Hz

Input Surge Current:
48 amps max.

Efficiency:
70% min. at full load with 115 VAC rms input

Output Voltages:
V1, +5.05 VDC
V2, +12 VDC CRT
V3, +12 VDC DISK
V4, −12 VDC

Output Power:
continuous 65 watts max.

Output Current:

	Output	Load Min.	Max.
Condition 1 (Model III use)	V1	1.35 A	4.0 A
	V2	0.60 A	1.5 A
	V3	0.40 A	2.1 A
	V4	0.005 A	0.10 A
Condition 2 (Hard Disk use)	V1	2.5 A	5.0 A
	V3	0.75 A	2.0 A*
	V4	0.005 A	0.10 A

***NOTE:** V2 and V3 connect in parallel to provide the V3 output. The V3 output will support a 5.0 A peak load which decays to 1.0 A in approx. 8 seconds. V1 and V3 must be within specified regulation when this surge decays to 4.0 A.

Output Ripple Voltage:

V1	(5.05 VDC)	50mV p-p
V2	(+12 VDC)	150mV p-p
V3	(+12 VDC)	150mV p-p
V4	(−12 VDC)	150mV p-p

NOTE: Ripple is the composite 100/120 Hz ripple due to the line, plus the high frequency ripple due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections should be ignored.

Output Voltage Regulation:
After initially setting V1, output voltage tolerances under all conditions of rated line, load, and temperature should remain within the following limits:

V1	(+5.05 VDC)	+/− 3%
V2	(+12 VDC)	see ***NOTE**
V3	(+12 VDC)	+/− 5%
V4	(−12 VDC)	+25%, −8.3%

***NOTE:** a) The initial value of V2 must not change by more than +/− 100mV under the following load conditions of V3:
— A step increase in output current from 0.4 A (initial condition) to 2.4 A, decaying within 60 msec to 2.1 A.
— A step decrease in output current from 2.1 A (initial condition) to 0.4 A.
b) V2 output voltage may vary +/− 5% under all other conditions of rated line, load, and temperature as defined in the specification.

Over-Current Protection:
Power supply will shut down before total power exceeds the point where damage would result. No damage will result when any output is short circuited continuously with 100 milliohms or less.

Over-Voltage Protection:
The +5.05 VDC circuit is protected with a "crowbar" circuit with a trip range of 5.8 to 6.8 VDC.

Hold-Up Time at Continuous Max Load:

Nominal Line	16 mSec minimum
Low Line	10 mSec minimum

5.4.3 Theory of Operation

The basic operating principles of a flyback converter and the necessary functional blocks to form a complete power supply were reviewed in the System Description section. In this part, the operation of each section of the circuit will be analyzed and later these sections will be connected to illustrate the signal flow in the power supply.

AC Input

A conventional bridge rectifier and a filter capacitor are connected directly across the AC line to provide the DC input voltage to the power supply.

Figure 5-38. Input AC Supply

An EMI filter consisting of capacitors C30-C33 and choke T2 are inserted at the input to the rectifier. This filter circuit keeps the high frequency signals generated in the power supply from being conducted into the AC power line. C30 and C31 provide a low impedance to the earth ground terminal for signals common to both hot and neutral sides of the AC line. C32 provides a low impedance dissipative path for the RF signal energy which appears across the line. T2 blocks RF signals common to both sides of the line and reflects them back toward the lower impedance elements near the rectifier. T2 also helps block differential (across-the-line) signals by using the EMF set up by the signal current on one side of the line to oppose the signal current flowing in the other side. C33 serves as a transient bypass capacitor to protect the power supply from large transient voltages that appear on the AC power line. C33 also improves the efficiency of the RFI filter choke T2 by terminating the line in a low impedance to absorb and dissipate any remaining differential RF energy.

R38 is a negative-temperature-coefficient-thermistor which limits the turn-on surge current of the power supply filter capacitor C29. The resistance of this thermistor when "cold" is approximately 10 ohms. As the filter capacitor charges toward the peak value of the AC input voltage, it draws less current from the line. At the same time, the heating effect of the current flowing in the thermistor causes its resistance to decrease until it reaches its rated "hot" resistance of less than 1 ohm. As you can see, the thermistor dissipates very little power when the power supply is in operation. The thermistor is designed to cool rapidly enough, during power loss or turn-off, to limit the turn-on surge after only a few seconds cool-down.

The fuse, a fast acting 3.0 amp unit, is selected to ignore the short term turn-on surges, but open quickly in the event of an abnormally high current that would result from a component failure in the DC input supply or current limiting circuits.

Auxiliary Power Supply

The auxiliary power supply is operational when the main supply is on and not in a shut-down condition. This power supply consists of winding 2-3 on T1, half-wave rectifier CR4, and filter capacitor C14. The voltage output is approximately +15 volts under normal conditions but momentarily reaches about +31 volts during start-up.

Kick Start Latch

Start up of the circuit is initiated by the kick start latch. This latch is shown in simplified form in Figure 5-39 (a) along with the accompanying waveforms in Figure 5-39 (b). When power is applied, C14 charges toward Vin = +160 volts through R26 with a time constant of approximately RC or 37.5 seconds. However, as we'll see, the kick start latch turns on in 2 or 3 seconds, the time required for the voltage across C14 to reach 30 + Vbe4 = 30.7 volts. At this point Q4 turns on and develops a bias across R21 which turns on Q5.

Referring to Figure 5-39b, as C14 dumps its charge into C1 beginning at time t2, the voltage across C14 starts to decrease toward a level that will be determined by the load composed of U1 and the base drive circuit. Notice that the voltage across C1 momentarily approaches the full 31 volts at time t3 before it drops down under load to about +15 volts at time t4.

Figure 5-39. Kick-Start Latch

With C1 charging rapidly through the low resistance of a saturated Q4 via Vbe5, the reference supply inside U1 develops its 5.0 volt output when the voltage across C1 exceeds about 8 volts. At this point, the supply has not quite yet started, but U1 has a DC supply at pin 10. All that remains is to start up the pulse generator so that the supply operates and replenishes the charge in C14 on each cycle, thus maintaining a DC source for U1 of about +15 volts. Completion of the start-up sequence occurs when the soft start circuit, described in the next section, has started the pulse generator.

Control Section

The control section consists of the control IC, the primary half of the feedback optocoupler U2, and the base drive circuit for the switching transistor. The control circuit IC has three major parts: an internal regulator, a pulse generator, and an error amplifier section.

The internal reference is a regulated +5.0 DC voltage. This voltage provides the reference voltages for the comparators used in the pulse generator as well as the DC supply voltage for the feedback optical coupler and the internal circuits of U1 except for its output transistors.

The pulse generator section of the control IC has four major parts: (a) sawtooth oscillator; (b) wave-shaping and output circuit; (c) regulating comparator; (d) dead-time comparator. Figure 5-40 illustrates the sawtooth oscillator and output circuit waveforms and the approximate levels of the DC control voltages applied by the comparators to the wave-shaping logic. The oscillator frequency is set by the values of R3 and C7 shown in Figure 5-41.

The amplitude of the sawtooth is set at 3.0 volts (approximately 60% of the 5.0 volt reference voltage). Whenever the sawtooth voltage, Vosc, exceeds both of the DC control voltages, Vreg and Vdt, the output circuit will be in the ON condition.

The DC control voltage, Vreg, set at a quiescent value by R6 and R9, varies in response to changes in the supply's DC output voltages as sensed by U3 and coupled through U2. Notice that these voltages will vary because of changes in output loading, AC input voltage, and also because of the residual 120 Hz ripple component from the main DC supply.

The dead-time control voltage, Vdt, is set at a constant value by R4 and R5 and ensures that the pulse generator "OFF" time will be at least 50% of the sawtooth period. This allows adequate time for the complete transfer of stored energy from the primary to the secondary of transformer T1 as discussed in the section on basic principles.

A concept known as duty cycle was introduced in earlier paragraphs. Duty cycle is defined as the ratio of the "ON" time of the sawtooth cycle to the total length of the sawtooth period. Since the sawtooth has a linear ramp characteristic, the duty cycle is also equal to:

$$\text{duty cycle } d = \frac{\text{Vosc, pk - Vreg}}{\text{Vosc, pk}} = \frac{\text{ton}}{\text{T period}}$$

There are three possible conditions of the duty cycle:

$d = 0$	which occurs when either control voltage Vreg or Vdt exceeds the peak value of the sawtooth waveform Vosc.
$d = 50\%$	which occurs when Vreg is less than Vdt. This happens when the loading on the output of the supply is heaviest and the AC input voltage is at its lowest permitted level (see specifications)
$0 < d < 50\%$	which occurs during normal operation.

The dead-time control voltage is used in one other important way. Notice the 4.7 ufd capacitor, C2, connected across R4 in Figure 5-41. When power is first applied to the supply, the voltage across the capacitor is zero. Therefore, Vdt = Vref = 5.0 volts and no pulses appear at the output because Vdt is greater than Vosc,pk. As C2 charges, Vdt decreases toward 1/2 (Vosc,pk) in a time determined by R5 and C2 as t = 5x15k ohm X 4.7 ufd = 1/3 second. As Vdt decreases past Vosc,pk, very narrow pulses begin appearing at pin 8 of U1. The pulses become successively wider until Vdt is less than Vreg. C2 continues charging until Vdt reaches the final correct value of about 1.5 volts. This action provides the soft start feature of the power supply and allows sufficient time for the DC input supply and latch to reach normal operating conditions before the supply is started. In effect, the load is connected to the supply gradually by the soft start circuit.

Figure 5-40. Oscillator, Pulse Generator Waveforms

Figure 5-41. Control Section

Frequency stability of the sawtooth oscillator is provided by the 2% tolerance and polyester construction of the timing capacitor, C7, and the 100 parts-per-million temperature stability and 1% tolerance of R3. Voltage stability of the DC control voltages is provided by the +/− 2 1/2 percent stability of the 5.0 volt reference.

The control section consists of two error amplifiers in U1, the primary half of U2, and associated circuitry shown in Figure 5-41. One of the error amplifiers serves as a regulator or pulse-width modulator which derives the DC control voltage, Vreg, from the signal voltage developed across R7 by the current in U2. This current is a replica of the current developed by U3 in response to the condition of the output voltage at the +5.1v and +12v outputs. This amplifier has a gain of about 10 determined by:

$$A = \frac{R8}{R9 \quad R6} = \frac{22k\ ohm}{2.35k\ ohm} = 10$$

The other error amplifier in U1 serves as a shut-down comparator. The positive terminal, pin 14, is set at the +5.0 volt reference and pin 13, the negative terminal or shut-down pin, is tied to the current limit latch. The output of this error amplifier (equal to Vreg since both error amplifier outputs are tied to the wave-shaping logic) will rapidly increase toward the +5.0 volts. Recall that if Vreg exceeds the peak sawtooth voltage, pulses are inhibited and the power supply shuts-down.

Base Drive

Figure 5-42 illustrates the BASE DRIVE circuitry which turns switching transistor Q7 on and off in response to the output of the pulse generator portion of U1. The "ON" circuit is shown in Figure 8a and the "OFF" circuit is shown in Figure 8b. Waveforms for these circuits appear in Figure 5-43.

The output transistor of U1 combined with Q3 forms a Darlington pair. This circuit provides the relatively large current necessary (through coupling capacitor C8) to turn on Q7. R23 limits this base current to a value large enough to turn on Q7 quickly, but not so large that it will exceed the ratings of Q3, C8, or the base emitter junction of Q7, or so large that the turn-off time of Q7 is excessive.

As Q3 turns on, C8 charges to approximately +5 volts and Q7 is driven into saturation. Energy is stored in the primary winding of T1 as the collector current of Q7 increases or "ramps up" at a rate determined by the inductance of the transformer primary winding.

When the output transistor of U1 turns off, the emitters of Q1 and Q2 are initially at the +6 volt level determined by the charge on C8, the Vbe drop of Q7, and the drop across R37. Both base-emitter junctions of the Q1-Q2 Darlington pair are biased ON and the positive terminal of C8 is clamped to near-ground by the saturating Q1. At this point, C8 still has most of its charge and the base voltage of Q7 is approximately −4.5 volts with respect to ground.

Figure 5-42. Base Drive Circuit

Figure 5-43. Q7 Base Voltage Waveform

With the strong reverse polarity provided by C8 across the base emitter junction of Q7, the "forward" charge stored in the junction capacitance is quickly swept out and Q7 is turned off. C8 continues to discharge through R24 to prepare for the next "ON" cycle. R19 limits the initial discharge of C8 while Q7 is turning off.

Notice the symmetry in the base drive circuit and the key role played by C8 in both the turn-on and turn-off sequences. Because of this crucial role in the circuit, this capacitor is specified as a high temperature, low-equivalent-series-resistance component.

Primary Circuit and Current Limit Shutdown

The Primary Circuit

The Primary circuit, shown in Figure 5-44 (a), functions exactly as described earlier in the "Basic Principle" section. That is, the switch (Q7) is controlled by the base drive waveform developed by the control section.

Figure 5-44. Primary Side Protection

The Snubber Circuit

Practical transformers cannot couple 100% of the stored energy from the primary to the secondary since all of the flux from the primary fails to link all the secondary turns. A circuit using this practical transformer behaves as though a small fraction of the primary inductance was not wound on the core of the transformer, but instead placed apart from the primary and in series with it. This small, separately-acting inductance does not participate in the transformer action and is called the leakage inductance.

If the resonant circuit, consisting of this leakage inductance and the stray capacitance in the adjacent circuit, has sufficient Q (relatively low resistance losses), a damped oscillation will occur in this resonant circuit when the transistor switch opens. The peak value of this oscillation will add to the Vce = 2 x Vin which appears across the transistor switch just after turn-off. The combined peak Vce may exceed the transistor breakdown rating if not damped out by the action of a snubber circuit.

When Q7 turns off, the energy stored in the leakage inductance is transferred to the electric field of the total capacitance of C37 plus stray capacitance. (Since C37 capacitance is much larger than the strays, it dominates in this action and tends to limit the peak value of the Q7 turn-off voltage.) If there were no resistance in this series connection of C37-plus-parasitics and leakage inductance, they would exchange this energy back and forth indefinitely. R40 is used to damp this oscillation without excessively slowing the turn-off voltage spike at the collector of Q7.

Current Limit Circuit and the Shut-Down Sequence

The current limit circuit forces the voltage level at a control pin of U1 to change to a near-zero value very quickly when the current in the transistor switch exceeds a predetermined point. It also removes the supply voltage from the control circuit and resets the kick start latch and soft-start circuits.

The current limit circuit shown in Figure 5-44(c) has three parts: a control bus, a detector, and a latch. The control bus supplies the operating DC voltage to the current limit circuit. It also conducts the current limit signal to control pin 13 and to the reset point in the kick start latch circuit. Diodes CR2 and CR3 steer this signal.

The normal maximum peak current in switching transistor Q7 is 3 amps. The detector transistor Q8 is biased to turn on by the divider action of R35 and R36 whenever the Q7 peak current through R37 exceeds 4 amps. A low-pass filter, formed by R35 and C22, prevents false detections on transient signals that don't represent an over-current condition.

As soon as Q9 turns on, its collector current develops the turn-on bias for Q8 across R33, and the Q8-Q9 pair "latches" in the "ON" state until the DC source for the latch is removed. Removal of this DC source occurs when C1 discharges through CR1, thus removing DC voltage from the control IC. Notice also that the kick start latch, Q4 and Q5, is still in the "ON" state and thus provides a discharge path for C14. When the decreasing voltage across C14 is less than approximately one volt, the Q4-Q5 latch also switches off.

At this point in time, all circuits are in an OFF condition except the input DC supply. C14 now begins to re-charge toward the input DC supply to restart the power supply. If a fault remains, the kick start and current limit circuits will continue to shut-down and re-start the power supply several times per second until the fault is removed or AC power to the supply is turned-off.

Under-Voltage Lockout

The Under-Voltage Lockout, UVL, shuts down the supply whenever the AC input voltage drops below about 90 volts. This occurs when the voltage at pin 13, set by the divider action of R27 and R25, diminishes to a level below the internal reference supply of the control IC. Pulses are inhibited immediately and because the DC supply to the Control IC is no longer replenished by the auxiliary supply, it discharges toward zero.

Why is it important to shut down the supply if the input AC line drops below 90 volts? The answer will become clear when an inherent characteristic of the circuit is discussed, namely, its negative input resistance.

Imagine the situation where the supply is delivering full power to its load and the AC input voltage drops five or ten volts. The supply control circuit responds by increasing the "ON" time of the switching transistor thus increasing the average current in the primary winding. The only way the DC supply can deliver more current is to draw it from the AC line. So the negative change in AC input voltage was accompanied by a positive change in AC input current.

Another way to describe this characteristic is that the supply is a constant power device, that is:

$$Pin = Vin \times Iin = constant.$$

Thus if V decreases, I will increase, and vice versa. The supply will thus draw more and more current from the AC line if the AC voltage continues to decrease. In order to limit the average current to a safe value, the control circuit senses the input voltage and shuts down the supply before the AC voltage level becomes too low or the AC current input becomes too high.

Secondary Outputs

Each of the secondary windings consist of a half-wave rectifier followed by a pi filter. The input capacitor of the filter stores the charge delivered to it when the rectifier is biased ON by the polarity of the transformer winding. The inductor and the output capacitor form a low-pass filter which removes the switching frequency ripple component.

The current output of the − 12 volt supply is much smaller than that of the positive voltage outputs. Because of this, the current limit circuit response is not sufficiently effective to prevent damage to the − 12 volt circuit. Therefore, a three terminal regulator with its own current limiting circuit is used to protect the − 12 volt output.

All of the 12-volt rectifiers are fast recovery types and the +5 volt rectifier is a Schottky type. These diodes feature high switching speeds during turn-off. Their low forward voltage drop minimizes dissipation resulting in maximum efficiency. Each of the positive outputs has a bleeder resistor.

The reason for two separate + 12 volt outputs is to provide sufficient isolation between different types of loads. It is easier to regulate the + 12 volts if the load which contains the DC motors in the disk drives is separated from the rest of the loads. In addition, the + 12 volt "Disk" output (V3) is included in the load sense network in order to minimize the load transients which occur when the disk drives turn on and off. The supply is then better able to regulate the other + 12 volt output (V2) during the severe V3 transitions.

Load Sense and Feedback Signal Development

The circuit of Figure 5-45 has three parts. In part (a), the IC's U2 and U3 are biased ON by resistors R11 and R22. These resistors also sense the changes in AC line input voltage to provide line regulation. U2A is the LED half of an optocoupler which serves to isolate the DC ground circuits of primary and secondary while coupling the AC feedback signal via optical coupling. U3 serves as both a stable DC reference voltage which the output voltages are compared against and as an error amplifier which provides the gain necessary for adequate sensitivity of the control IC to load changes.

Figure 5-45. Feedback Signal Development

Each of the passive components in the load sensing network is a high stability (+/− 100ppm) part to assure stability of the network over the operating temperature range of the power supply.

Part (b) of Figure 5-45 includes the network which tailors the frequency response of the error amplifier so that it responds to low frequency change only. This network, consisting of R14/C5 and R13/C4, also determines the stability of the power supply by ensuring that the power supply control circuit has no tendency to oscillate.

Part (c) illustrates the load sensing network. Equal currents through R15 are supplied from the +12V DISK and +5.05V outputs by R29 and R30. In addition, a portion of the transient signal occurring on the +12V CRT output (when the motors turn on or off) is fed to R15 by C17. The wiper of R15 feeds a control signal which represents the status of the current loads to the error amplifier U3. U3 amplifies and compensates it then U2 couples that control signal to U1 where it is used to vary the switching transistor (Q7) ON time to adjust the output voltages as necessary. R15 is adjustable to provide the initial set-up of the +5.05V output when it is installed in a computer.

Figure 5-46. Overvoltage Crowbar

Overvoltage Crowbar

Some of the circuits supplied by the +5 volt output are quite sensitive to voltages in excess of 7 volts. Since some circuits require both +5 and +12 volts, a failure in those circuits could apply +12 volts to the +5-volt bus and thus damage some of the +5-volt circuits. To prevent the +5-volt bus from exceeding a safe level, an SCR, Q6, is used to "crowbar" or short-circuit the +5.05 volt output to the secondary ground bus. This short circuit triggers the current limiting circuit and the supply shuts down until it tries to restart.

Referring to Figure 5-46, VR2 sets the turn-on point of the SCR and R17 develops the gate signal when VR2's Zener breakdown voltage of 5.6 volts is exceeded. C6 and R17 provide current limiting for VR2 and filter the gate signal so Q6 won't respond to transient signals.

Power Chain

In a sense we have already analyzed the power chain in the section on basic principle of operation. The base drive causes the switching transistor to turn on and off at a prescribed rate. This action alternately stores energy from the DC input in the primary inductance and releases it into the secondary through the flyback transformer action. The energy is then stored in the input filter capacitor at a voltage determined by the transformer turns ratio. Notice that the turns ratio determines the ratio of collector voltage to secondary voltage, both of which are alternating voltages. The ratio of input-to-output DC voltage is determined by the duty cycle and the turns ratio together.

For example, let's look at the +5 volt output of Figure 5-31 at normal loading and approximtely 120 VAC input. Under these conditions, the DC input voltage is 168 VDC and the duty cycle is approximately 40%. Thus, our average DC voltage at the switching transistor collector (or across the primary) is 40% of 168 or 67.5 volts. Dividing this average DC voltage by the turns for the 5 volt secondary (54 : 4 = 13.5) gives us 5.0 volts.

Figure 5-47. Power Chain

Control Chain

Imagine the load end of the feedback path disconnected from the +5.05 volt output terminal and unfolded so that the load sense network is now at the "input". The secondary rectifier (CR5) and filter (C10-C12, L1,) remain as the output. The circuit as it now appears, redrawn in simplified form in Figure 5-48, is known as the control chain. To see how the regulation action occurs, assume a small negative voltage change at the "input" of the feedback network and follow it through the control chain.

This negative voltage change, which would correspond to a slightly heavier load current, appears at pin 1 of U3 as a decreasing voltage. The error amplifier in U3 inverts and amplifies this signal. The positive-going output voltage of U3 at pin 3 causes less current to flow in the internal LED of U2A. A replica of this smaller current, optically coupled and induced in the phototransistor of U2B, develops a reduced voltage across R7 at the non-inverting input of the regulator error amplifier in U1.

The regulator error amplifier in U1 does not invert the signal, but further amplifies it, improving the sensitivity of the control chain to small changes at the power supply output. The regulator error amplifier output is Vreg. Since we established earlier that a negative-going Vreg increases the length of the base drive pulse, Q7 is turned on a little sooner so that it can store more energy from the AC line in the primary inductance. Finally, this increased energy is stored in the filter capacitor C10, C11 during the flyback interval and supplies the increased demand for current that resulted in the original reduction in the output voltage.

More simply stated, the control chain uses an amplified version of the output voltage CHANGE to adjust the width of the base drive pulse through the action of a control voltage at a comparator input.

Figure 5-48. Control Chain Simplified Schematic

5.4.4 Troubleshooting Chart for 65 Watt Power Supply

Trouble	Cause	Remedy
open fuse	shorted line input filter capacitor	check and/or replace C33, C32, C31, C30
	shorted bridge	check BR1
	shorted filter capacitor	check C29, C26, R39
	shorted switching transistor	check Q7, C37, R40, C26, T1 pri., Q3, Q1, R37
Current limit cycle	single rectifier open in bridge	check and/or replace BR1
	open filter capacitor	check C29
	shorted snubber capacitor or resistor	check C37, R40
	open opto-coupler	check U2
	shorted supply output	check computer for short on +5V, +12V CRT, +12V DISK, −12V outputs and clear shorted condition
	shorted output rectifier	check CR5, CR6, CR7, CR8
	open or shorted output filter capacitor	check C16, C18, C25, C23, C10, C11, C12, C19, C20
	defective crowbar	check Q6
no pulses at pin 8 of U1, (i.e., supply shut down)	no aux. DC supply	Check and/or replace CR4, C14, T1 aux.
	no "kick start"	check R26, Q4, Q5, VR1, CR1, C1
	no base drive	check U1, Q3, R23, C8, R24
	dead-time control divider malfunction	check C2, R4, R5, U1 (for V ref.)
	under-voltage protect divider malfunction	check R27, R25, C9, Q9
	PWM feedback malfunction	check and/or replace U1, U2, C3

5.4.5 Testing and Adjustments

The following tests should be performed to guarantee correct operation of the power suply after repairs have been made. The first test checks the primary circuits and is to be made without AC power applied. The second test is a complete operational test with AC power applied.

Primary, Checks T2, U1

NO AC POWER APPLIED

1. Apply +35 volts DC via 170 ohm, 5 watt resistor from Q4 emitter to the primary side of ground. Primary side ground is the point labeled 1 on the schematic. Also apply 35 volts DC via a 120k ohm resistor and a normally closed SPST switch from Pin 13 of U1 to primary ground. Observe the voltage across C14 as it charges. As it reaches a value near +31 volts, it should drop to near +16 volts as Q5 and U1 turn on.

2. Check U1 pin 8 and/or Q7 base for a base drive pulse: a 40 kHz square wave of 8/4 volts respectively.

3. Switch the SPST switch connecting the 120k ohm resistor from Pin 13 of U1 and check for loss of base drive pulses on Q7.

Operational, Checks T2, U1, U2

APPLY AC POWER

1. Apply rated maximum loading for condition 1 (Model III use) or condition 2 (5 1/4" Hard Disk use).

2. Apply 120 VAC input voltage and observe Q7 current (via loop on PCB) and voltage (at TP2). Supply should start in two to four seconds.

3. Observe the +5.05 olt output and adjust R15 until the output is exactly +5.05 volts DC.

4. Measure +12V and −12V outputs.

5. Check all outputs at Vin = 90 VAC and 135 VAC at:
   (a) minimum and maximum loads
   (b) check +12V CRT when +12V DISK varies in transient test.

6. Measure ripple. See Measurement Techniques below.

7. Measure efficiency. See Measurement Techniques below.

8. Test operation of current limit and over-voltage protection circuits by applying +7.0 volts to the +5 volt output.

Measurement Techniques

1. Ripple — Unit connected to full load at low line. One end of 50 ohm coaxial cable connected to output terminals. Other end of cable (terminated with 0.01uF ceramic cap in series with 51 ohm resistor) connected to scope using BNC T-fitting. Two components at 120 Hz and 40 kHz.

2. Efficiency — Use Diego Systems Series 200 power monitor.

$$\text{Efficiency} = \frac{\text{Power Out}}{\text{Power In}}$$

REVISION
ZONE
LTR
DESCRIPTION
DATE
APPROVED
RELEASED FOR PRODUCTION
2-14-84
POWER CORD
18 AWG
3 COND
LINE
EARTH
NEUTRAL
POWER CONNECTOR
18 AWG
BRN(LINE)
GRN/YEL (CHASSIS)
BLU(NEUTRAL)
POWER SWITCH
250V / 11A
BRN (LINE)
18AWG
BLU (NEUTRAL)
65W SWITCHING POWER SUPPLY
FUSE
2.5A/250V
N
TO CHASSIS THROUGH MOUNTING SCREW
MAIN PCB
+5VDC / RED / 20AWG
+12VDC / ORG / 22AWG
-12VDC / WHT / 22AWG
GROUND / BLK / 20AWG
DISK DRIVES
+5VDC / RED / 20AWG
+12VDC / ORG / 20AWG
GROUND / BLK / 20AWG
MONITOR
RED +12VDC / VIO / 18AWG
GROUND / BLK / 18AWG
MODEM PCB
+5VDC / RED / 20AWG
+12VDC / ORG / 20AWG
-12VDC / WHT / 20AWG
GROUND / BLK / 20AWG
FAN
12VDC
+12VDC / ORG / 20AWG
GROUND / BLK / 22AWG
DRAWN
DAN CRONCH
12/5/84
CHECKED
DESIGN
APPROVED
SCHEMATIC —
POWER DISTRIBUTION,
MODEL 4P,
PROJECT 509
tandy
DWG NO
8000221
SIZE
C
SCALE
N/A
SHEET
1
OF
1

WAVEFORMS

See schematic notations.
→ = 0 reference

Ⓐ 50 mv/d vert.
5 μ/d horiz. AC

Ⓑ 50 v/d vert.
5 μ/d horiz. DC

Ⓒ 1 v/d vert.
5 μ/d horiz. DC

Ⓓ 1 v/d vert.
5 μs/d horiz. DC

Ⓔ 1 v/d vert.
5 μs/d horiz. DC

Ⓕ 5 v/d vert.
5 μs/d horiz. DC

Ⓖ 0.2 v/div vert.
5 μs/d horiz. DC

TANDY CORP.

65W POWER SUPPLY

REDUCE TO 8.500±.010

REDUCE TO 5.500±.010

REDUCE TO 5.500±.005

TANDY CORP.

65W POWER SUPPLY

REDUCE TO 8.500±.005

PARTS LIST

Power Supply Assembly 8790049, 65W

Item	Sym	Description	Part Number
1	1	Printed Circuit Board	8709365
1	J1	Fan Output 2-pin verticle	8519214
	BR1	Bridge, 2A, 600PIV	8160402
	C1	10µF, 35V, elect., radial	8326103
	C2	4.7µF, 50V, elect., radial	8325474
	C3	0.047µF, 50/63V stacked metal	8393474
	C4	0.47µF, 50/63V stacked metal	8394474
	C5	0.068µF, 50/63V stacked metal	8393684
	C6	1µF, 50, elect., radial	8325014
	C7	0.001µF, 63V poly	8392104
	C8	47µF, 25V, elect., radial	8326472
	C9	1µF, 50V, elect., radial	8325014
	C10	2200µF, 10V, elect., radial	8328224
	C11	2200µF, 10V, elect., radial	8328224
	C12	2200µF, 6.3V, elect., radial	8328220
	C13	0.01µF, 50/63V stacked metal	8393104
	C14	100µF, 35V, elect., radial	8327103
	C15	1000pF, 100V, ceramic disc	8302106
	C16	2200µF, 16V, elect., radial	8328221
	C17	0.1µF, 50/63V stacked metal	8304104
	C18	3300µF, 16V, elect., radial	8328331
	C19	100µF, 35V, elect., radial	8327103
	C20	100µF, 25V, elect., radial	8327102
	C21	.047µF, 50/63V stacked metal	8393474
	C22	.01µF, 50/63V stacked metal	8393104
	C23	470µF, 16V, elect., radial	8327461
	C24	0.1µF, 250VDC metal poly	8394106
	C25	2200µF, 16V, elect., radial	8328221
	C26	220µF, 200V, elect., radial	8327226
	C27	Not Used	
	C28	4700 pF, 125VAC, ceramic disc	8303475
	C29	220µF, 200V, elect., radial	8327226
	C30	4700pF, 125VAC, ceramic disc	8303475
	C31	4700pF, 125VAC, ceramic disc	8303475
	C32	.22µF, 125VAC, ceramic disc	8393432
	C33	.01µF, 250VAC, metal paper	8393106
	C34	Not Used	
	C35	Not Used	
	C36	.001µF, 50/63V stacked metal	8392014
	C37	.001µF, 630V, poly	8392017
	C38	.022µF, 63V, poly	8393422

PARTS LIST

Power Supply Assembly 8790049, 65W

Item	Sym	Description	Part Number
	C39	.022µF, 63V, poly	8393422
	CR1	Diode, 1N4148, switching	8150148
	CR2	Diode, 1N4002, 1A/50PIV	8150002
	CR3	Diode, 1N4002, 1A/50PIV	8150002
	CR4	Diode, 1N4934, 1A/100PIV	8150934
	CR5	Diode, MBR1035, 8/10A, 35V, TO-220	8150035
	CR6	Diode, MUR810, 8A/100PIV, TO-220	8150810
	CR7	Diode, 1N4934, 8A/100PIV	8150934
	CR8	MUR810, 8A/100PIV, TO-220	8150810
	CR9	Not Used	
	CR10	Diode, 1N4002, 1A/50 PIV	8150002
	CR11	Diode, 1N4002, 1A/50 PIV	8150002
	F1	3 amp, AGC	8479104
	L1	Inductor, 5.0µh, 10A	8419006
	L2	Inductor, 30µh, 5A	8419008
	L3	Not Used	
	L4	Inductor, 30µh, 5A	8419008
	L5	Inductor, 100µh, 3A	8419009
	Q1	Transistor, MPSU51A, PNP, TO-202	8100051
	Q2	Transistor, MPSA55, PNP, TO-92	8100055
	Q3	Transistor, MPSU01A, NPN, TO-202	8111001
	Q4	Transistor, MPSU51A, PNP, TO-202	8100051
	Q5	Transistor, MPSU01A, NPN, TO-202	8111001
	Q6	SCR, 8A/50PIV, TO-220	8140122
	Q7	Transistor, MJE13006, NPN, 8A, 400V	8110006
	Q8	Transistor, MPSA55, PNP, TO-92	8100055
	Q9	Transistor, MPSA05, NPN, TO-92	8110005
	U1	IC, MC34060 Switching Regulator or	8060060
		IC, µA/TL494 Switching Regulator	8060494
	U2	IC, Opto-isolator, 4N35	8170035
	U3	IC, µA/TL431, Positive Shunt Reg.	8060428
	R1	Resistor, 1K, 1/4W, 5%	8207210
	R2	Resistor, 68 ohm, 1/4W, 5%	8207068
	R3	Resistor, 28K, 1/4W, 1%	8200328
	R4	Resistor, 39K, 1/4W, 5%	8207339
	R5	Resistor, 15K, 1/4W, 5%	8207315

PARTS LIST

Power Supply Assembly 8790049, 65W

Item	Sym	Description	Part Number
	R6	Resistor, 4.7K, 1/4W, 5%	8207247
	R7	Resistor, 10K, 1/4W, 5%	8207310
	R8	Resistor, 22K, 1/4W, 5%	8207322
	R9	Resistor, 4.7K, 1/4W, 5%	8207247
	R10	Resistor, 4.7K, 1/4W, 5%	8207247
	R11	Resistor, 100 ohm, 1/4W, 5%	8207110
	R12	Not Used	
	R13	Resistor, 18K, 1/4W, 5%	8207318
	R14	Resistor, 330 ohm, 1/4W, 5%	8207133
	R15	1K, 20%, linear Pot.	8279211
	R16	Resistor, 3.32K, 1/4W, 1%	8200232
	R17	Resistor, 100 ohm, 1/4W, 5%	8207110
	R18	Resistor, 10 ohm, 1/4W, 5%	8207010
	R19	Resistor, 1 ohm, 1/4W, 5%	8207001
	R20	Resistor, 10K, 1/4W, 5%	8207310
	R21	Resistor, 150 ohm, 1/4W, 5%	8207115
	R22	Resistor, 330 ohm, 1/4W, 5%	8207133
	R23	Resistor, 27 ohm, 2W, 10%	8248127
	R24	Resistor, 22 ohm, 1/2W, 5%	8217022
	R25	Resistor, 22K, 1/4W, 5%	8207322
	R26	Resistor, 56K, 1W, 5%	8247356
	R27	Resistor, 390K, 1/4W, 5%	8207439
	R28	Resistor, 22 ohm, 1/4W, 5%	8207022
	R29	Resistor, 28K, 1/4W, 1%	8200328
	R30	Resistor, 6.65K, 1/4W, 1%	8200266
	R31	Not Used	
	R32	Resistor, 1K, 1/4W, 5%	8207210
	R33	Resistor, 100 ohm, 1/4W, 5%	8207110
	R34	Resistor, 1K, 1/4W, 5%	8207210
	R35	Resistor, 68 ohm, 1/4W, 5%	8207068
	R36	Resistor, 100, 1/4W, 5%	8207110
	R37	Resistor, 0.22 ohm, 2W, 10%	8248022
	R38	Thermistor 10 ohm 25c	8298010
	R39	Resistor, 56K, 1W, 5%	8248356
	R40	Resistor, 82 ohm, 5W, 5%	8248082
	R41	Resistor, 56K, 1/4W, 5%	8207356
	R42	Resistor, 4.7K, 1/4W, 5%	8207247
	T1	Transformer, Power, 65W flyback	8790063
	T2	Line Choke, 5.5mH/side, 2A	8790045
	VR2	Zener, 1N5232B, 5.6V	8150232
	VR1	Zener, 1N5256B, 30V	8150256
	VR3	Voltage Regulator 79M12 -12V	8051912

MISCELLANEOUS HARDWARE

2	Clip, Fuse, PC Mount 1/4" Fuse (F1)	8559042
1	Connector, 2 Pin, Vert. (J1)	8519214
1	Connector, 3 Pin (J3)	8519153
1	Connector, 13 Pin (J2)	8519154
1	Bracket, Heatsink, TO-220 (CR5,6,8)	8729167
1	Heatsink, Transistor, TO-220 (Q7)	8549003
4	Insulator, TO-220, Mica (Q7,CR5,6,8)	8539003
4	Nut, KEPS, #4-40 (Q7,CR5,6,8)	8579003
4	Screw, #4-40 x 3/8" (Q7, CR5,6,8)	8569002
4	Washer, Shoulder (Q7, CR5,6,8)	8589026
4	Wire, Jumper 20 Ga. (W1,2,5,6) .5"	
1	Wire, Jumper 20 Ga. (W7)	
1	Wire, Jumper 20 Ga. (W4)	
1	Wire, Stranded 600V (W3)	8433006

5.5 CRT DISPLAY

5.5.1 Specifications

The supply voltage is 12.000 DC, +/−0.10V, from a regulated power supply. The room temperature is 25 degrees C.

		Unit	Nominal	Limit
Power Input (1K=30uA),12V		(A)	0.85	1.0
Input Level				
Horizontal (Positive-going Sync)		(V)	–	TTL Compatible
Vertical (Negative-going Sync)		(V)	·	TTL Compatible
Video (Positive-White)		(V)	–	TTL Compatible
Video Bandwidth (10Hz - 12MHz)		(dB)	–	+/− 3
Horizontal Retrace		(μSec)	8.2	9.5
Vertical Retrace		(μSec)	700	1,000
Scanning Frequency				
Horizontal		(Hz)	15,840	+/−500
Vertical		(Hz)	–	47 - 63
Resolution at Center		(Lines)	–	800
Resolution at Corner		(Lines)	–	680
Geometric Distortion				
Pin/Barrel distortion on top/bottom		(Inch)	–	+/−0.05
	on Sides	(Inch)	–	+/−0.038
Trapezoidal Distortion top/bottom		(Inch)	–	0.150
	left/right	(Inch)	–	0.100
Parellogram Distortion		(Inch)	–	0.100
Raster Tilt		(Degree)	–	+/− 1.0
Linearity		(%)	–	+/−10
Vertical Size				
Video (24 rows)		(Inch)	4.5	+/−0.20
Horizontal Size				
Video (80 characters/Row)		(Inch)	6	+/−0.20

Figure 5-49. Video Monitor 8790613 (612)

5.5.2 Adjustment Procedures

Horizontal Synchronization Adjustment (Figures 5-50 thru 5-52)

When there is a pattern on the CRT as shown in Figure 5-50, 5-51, adjust VR301 to terminate scrolling, and then do VR301 slightly to move the video into the center of the raster as illustrated in Figure 5-52.

Figure 5-50.

Figure 5-51.

Figure 5-52.

Vertical Synchronization Adjustment (Figures 5-53, 5-54)

Adjust VR201 to stop scrolling, when video is rolling upward or downward as shown in Figure 5-53. By turning VR201 clockwise and counter-clockwise, the initial points of scrolling can be confirmed. Consequently, set VR201 at the center between the confirmed points.

Figure 5-53.

Figure 5-54.

Vertical Size Adjustment (Figure 5-55)

Generate a full white screen on the CRT, and adjust the video's vertical size to be 4.5".

Figure 5-55.

Horizontal Size Adjustment (Figure 5-56)

Generate a full white screen on the CRT. Adjust video's horizontal size with L302 to be 6.0".

Figure 5-56.

Focus Adjustment (Figure 5-57)

Display a full screen of the character "H" and adjust VR303 so that all the characters are the same size and shape and in sharp focus. While adjusting, observe both peripheral and central areas of the display.

Figure 5-57.

Raster Tilt Adjustment (Figures 5-58, 5-59)

Form a series of " – " characters along the horizontal center line as shown in Figure 5-58. Adjust the center line to make A1 = A2 by turning the deflection yoke left and right.

Figure 5-58.

Note: Loosen the cramp screw on the deflection yoke for tilt adjustment as shown in Figure 5-59.

Figure 5-59.

Video Centering Adjustment (Figure 5-60)

Display a white screen or a full screen of the character "H" and adjust the centering magnet on the deflection yoke to make L = R and T = B.

Figure 5-60.

Internal Brightness Adjustment (Figure 5-61)

Set the remote brightness control to the center position, and adjust VR302 to hold the raster at the point at which it is first visible.

Figure 5-61.

Video Distortion Adjustment (Figures 5-62, 5-63)

Insert a video distortion-correcting magnet onto the magnetic holder if required, and rotate it for adjustment.

Pincushion/Barrel Correction (Top, Bottom and Sides)

Perform this adjustment if the CRT exhibits the abnormal effects shown in Figure 5-62.

Step 1. Push the magnet on the yoke mounting pin as shown Figure 5-63. A magnet should be placed only on the pin that corresponds to the affected area.

Step 2. Rotate the magnet to obtain the desired video display labeled "NORMAL" on Figure 5-62.

Step 3. If the desired video display cannot be obtained, replace with a proper magnet.

Figure 5-62.

Trapezoidal Correction (Corners) Procedure

Perform this adjustment if the CRT exhibits the abnormal effects as shown in Figure 5-63.

Step 1. Push a magnet onto the yoke mounting pin as shown in Figure 5-63. Magnet should be placed only on the pin that corresponds to the affected area.

Step 2. Rotate the magnet to obtain the desired video display, labeled "NORMAL" in Figure 5-63.

Step 3. If the desired video display cannot be obtained, replace with a proper magnet.

Figure 5-63.

5.5.3 Theory of Operation

Video Control
The DC controlling voltage from P8 determines the level of TTL compatible, positive and non-composite video signal which is provided by the CPU.

Video Drive and Video Out
Q102 and Q103 are connected in a cascade configuration. The video signal, of which the level is subject to the video control as stated above, comes into the base of Q102. C102 and R105 compensate high frequency. The video out signal (with flat response) is amplified via Q103 and provided to the cathode of CRT501.

The Vertical Control Process
The vertical control process consists of four stages: Vertical Oscillator, Vertical Drive, Vertical Out and Flyback Generator. These four stages are processed by IC201.

Vertical Oscillator
A sawtooth wave pattern is generated through C204, R204, VR201 and an oscillator circuit, and synchronized with the negative-going vertical sync signal which is applied to pin 1 of IC201.

Vertical Drive
A vertical sawtooth wave is AC coupled to the vertical drive amp for linear amplification via C207.

Vertical Out
The vertical drive is linked to vertical out within IC 201. Vertical output from Pin 8 of IC201 is applied to DY501, and is AC coupled by C209. Part of the output power at R206 is returned to a vertical drive by the NF loop which is made up of C205, C206, R207, and VR202, providing lineality compensation to the electric current which passes across the deflection yoke.

Flyback Generator
A pulse that exceeds the source voltage (=20V) is generated at the vertical output terminal, Pin 8 of IC201, during retrace. The Flyback pulse generator which consists of D201, C211 and a part of IC201 boosts the source voltage for that period accordingly.

Horizontal Sync Amp
A TTL compatible, positive-going horizontal drive signal from P-6 is wave-shaped by C301 and R301, amplified by Q301 and applied to the Pin 1 of IC301.

Phase Detector
The negative-going horizontal pulse is applied to a filter that consists of R306, C306 and C310, used as a sawtooth wave for comparison and is AC coupled via C305 and flows to Pin 3 of IC301. The retrace part of horizontal sawtooth wave and the horizontal sync signal are applied to a phase detector and exist on Pin 4 of the phase detector. This output is used for the phase control of DC through the filter, consisting of C307, C308 and R305.

Horizontal Oscillator
A horizontal pulse is provided through the horizontal oscillator circuit consisting of C311 and IC301. This oscillator signal is phase-controlled according to the signal from the phase detector out (Pin 4 of IC301). The horizontal oscillator frequency is adjusted by VR301.

Horizontal Drive
The horizontal oscillator output (which is phase-controlled as stated above), is applied to the horizontal drive buffer for amplification through IC301, and goes out on Pin 7 of IC301.

X-Ray Protection
When supplied with excessive source voltage (more than about 14V), the X-ray protection of IC301 works to terminate the horizontal oscillator to prevent the CRT from emiting X-rays over the regulated amount. High voltage causes CRT's to emit more X-ray radiation than allowed.

Horizontal Out
Output power at Pin 7 of the horizontal control process IC is applied to Q303 through T301. Q303 operates a switching function with about 21μ sec OFF and 42μ sec ON. An electrical current of sawtooth waves comes to DY501 through Q303 actuating a switching function and a dumper-diode, which helps to deflect the electron beams.

Electrical current passes across DY501. This pulse voltage is enhanced by the FBT, rectified, and used as the anode voltage (11kV), focus voltage (450V) or video voltage (60V).

The output pulse at the collector of Q303 is rectified to be doubled (−160V) and provided as the voltage for internal brightness and focus.

AN5763 IC201

BLOCK DIAGRAM

AN5753 IC301

BLOCK DIAGRAM

Figure 5-64.

DEFLECTION P.C.B. TOP VIEW

Parts List

9" Video Monitor 879Ø612, Model 4P Computer

Item	Sym	Description	Part Number
	1	PCB Assembly, CRT	U31ØØ5
	1	Clip, Fuse	1973Ø3Ø8ØA
	1	Connector, Pin	19411Ø78ØA
	1	Fuse, 2A 25ØV	251ØØØ79ØA
	1	Spring, Tension	434Ø1Ø12ØA
	1	Socket, Pin	194Ø1Ø37ØA
	1	Socket, Cylindrical	19631ØØ1ØA
	1	Cord, Terminal	316Ø1Ø15ØB
	1	Cord, Terminal	316Ø1Ø14ØA
	C1Ø1	Capacitor, 4.7 uF, 5ØV Elec 2Ø%	CEØ4(RB)475M5ØV
	C1Ø2	Capacitor, 12Ø pF, 5ØV Cer 1Ø%	CK45B1H121K
	C1Ø3	Capacitor, Ø.1 uF, 5ØV Mylar 1Ø%	CQ92M1H1Ø4K
	C1Ø4	Capacitor, 22 uF, 1ØØV Elec 2Ø%	CEØ4C226M1ØØV
	C1Ø5	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C2Ø1	Capacitor, Ø.Ø22 uF, 5ØV Mylar 1Ø%	CQ92M1H223K
	C2Ø2	Capacitor, Ø.Ø22 uF, 5ØV Mylar 1Ø%	CQ92M1H223K
	C2Ø3	Capacitor, Ø.Ø1 uF, 5ØV Mylar 1Ø%	CQ92M1H1Ø3K
	C2Ø4	Capacitor, Ø.33 uF, 16V Tant 1Ø%	CS15E1C334K
	C2Ø5	Capacitor, 4.7 uF, 16V Tant 1Ø%	CS15E1C475K
	C2Ø6	Capacitor, 4.7 uF, 16V Tant 1Ø%	CS15E1C475K
	C2Ø7	Capacitor, 33 uF, 16V Elec 2Ø%	CEØ4C336M16V
	C2Ø8	Capacitor, 33 uF, 16V Elec 2Ø%	CEØ4C336M16V
	C2Ø9	Capacitor, 33Ø uF, 35V Elec 2Ø%	CEØ4C337M35V
	C21Ø	Capacitor, Ø.Ø33 uF, 5ØV Mylar 1Ø%	CQ92M1H333K
	C211	Capacitor, 22Ø uF, 16V Elec 2Ø%	CEØ4C227M16V
	C212	Capacitor, 1ØØ uF, 16V Elec 2Ø%	CEØ4C1Ø7M16V
	C3Ø1	Capacitor, 22Ø pF, 5ØV Cer 1Ø%	CK45B1H221K
	C3Ø2	Capacitor, Ø.47 uF, 5ØV Elec 1Ø%	CEØ4(RB)474K5ØV
	C3Ø3	Capacitor, 1ØØ pF, 5ØV Cer 1Ø%	CK45B1H1Ø1K
	C3Ø4	Capacitor, Ø.Ø22 uF, 5ØV Mylar 1Ø%	CQ92M1H223K
	C3Ø5	Capacitor, Ø.Ø18 uF, 5ØV Mylar 1Ø%	CQ92M1H183K
	C3Ø6	Capacitor, Ø.Ø18 uF, 5ØV Mylar 1Ø%	CQ92M1H183K
	C3Ø7	Capacitor, 4.7 uF, 5ØV Elec 2Ø%	CEØ4C475M5ØV
	C3Ø8	Capacitor, Ø.Ø1 uF, 5ØV Mylar 1Ø%	CQ92M1H1Ø3K
	C3Ø9	Capacitor, 22Ø uF, 16V Elec 2Ø%	CEØ4C227M16V
	C31Ø	Capacitor, 1ØØ pF, 5ØV Cer NPO	CC45CH1H1Ø1J
	C311	Capacitor, Ø.ØØ47 uF,5ØV Poly 5%	CQ92P1H472J
	C313	Capacitor, 1ØØØ uF, 25V Elec 2Ø%	CEØ4C1Ø8M25V
	C314	Capacitor, Ø.Ø33 uF, 4ØØV Poly 5%	CQ92P2G333J
	C315	Capacitor, Ø.Ø47 uF, 4ØØV Poly 1Ø%	CQ92P2G473K
	C316	Capacitor, 1 uF, 25ØV Elec 2Ø%	CEØ4C1Ø5M25ØV
	C317	Capacitor, Ø.Ø1 uF, 63ØV Poly 1Ø%	CQ92P2J1Ø3K

VIDEO MONITOR

DEFLECTION P.C.B. BOTTOM VIEW

CRT P.C.B. TOP VIEW

CRT P.C.B. BOTTOM VIEW

NOTE (1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" ($K=10^3$ OHM, $M=10^6$ OHM)
(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" ($P=10^6$ μF)

ISSUED
OCT. 11. 1983
TC ELECTRONICS ENG. DEP.

Revised on May 16, 1983

APPROVED BY	TITLE	
3/7/83	SCHEMATIC DIAGRAM	
CHECKED BY 1983/3/8	MODEL	DRAWING NO.
DESIGNED BY 1983/1/18	VIDEO MONITOR 8790612	D-23533

NOTE (1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" (K=10³ OHM, M=10⁶ OHM)
(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" (P=10⁻⁶ μF)

APPROVED BY	TITLE	
CHECKED BY	SCHEMATIC DIAGRAM	
DESIGNED BY	MODEL: VIDEO MONITOR 8790613	DRAWING NO.: D-23757

Parts List

9" Video Monitor 879Ø612, Model 4P Computer

Item	Sym	Description	Part Number
	C318	Capacitor, Ø.Ø1 uF, 63ØV Poly 1Ø%	CQ92P2J1Ø3K
	C319	Capacitor, Ø.ØØ47 uF, 1ØØØV Cer	CK45E3A472P
	C32Ø	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C321	Capacitor, Ø.ØØ22 uF, 1ØØØV Cer	CK45E3A222P
	C322	Capacitor, 1Ø uF, 25V Elec 2Ø%	CEØ4(RP)1Ø6M25V
	C323	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C324	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C35Ø	Capacitor, Ø.ØØ82 uF, 4ØØV Poly 5%	CQ92P2G822J
	C4Ø1	Capacitor, 22Ø uF, 16V Elec 2Ø%	CEØ4C227M16V
	C5Ø1	Capacitor, Ø.ØØ1 uF, 1ØØØV Cer	CK45E3A1Ø2P
	D1Ø1	Diode, 1ØE-1, Silicon	1ØE-1
	D2Ø1	Diode, 1ØE-1, Silicon	1ØE-1
	D2Ø2	Diode, VD1221, Varistor	VD1221
	D2Ø3	Diode, VD1221, Varistor	VD1221
	D3Ø2	Diode, BBT4, Silicon	BBT4
	D3Ø3	Diode, BBT4, Silicon	BBT4
	D3Ø4	Diode, BBT4, Silicon	BBT4
	D3Ø5	Diode, BBT1Ø, Silicon	BBT1Ø
	D3Ø6	Diode, BBT4, Silicon	BBT4
	DY5Ø1	Deflection Yoke	58151ØØ3ØA
	IC2Ø1	IC, AN5763, Linear V-Processor	AN5763
	IC3Ø1	IC, AN5763, Linear H-Processor	AN5763
	L3Ø1	Coil, 1Ø uH, Linearity	14341ØØ4ØA
	L3Ø2	Coil, 3Ø uH, Width	14331Ø14ØA
	R1Ø1	Not used	
	R1Ø2	Resistor, 15 kohm, 1/4W 5% Carbon	RD1/4MB(S)153J
	R1Ø3	Resistor, 1 Mohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø5J
	R1Ø4	Resistor, 22Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)221J
	R1Ø5	Resistor, 33 ohm, 1/4W 5% Carbon	RD1/4MB(S)33ØJ
	R1Ø6	Resistor, 91 ohm, 1/4W 5% Carbon	
	R1Ø7	Resistor, 47 kohm, 1/4W 5% Carbon	RD1/4MB(S)473J
	R1Ø8	Resistor, 1 kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø2J
	R1Ø9	Resistor, 1 kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø2J
	R11Ø	Resistor, 1.5 kohm, 3W 5% Met Oxide	RSM3P152J
	R111	Resistor, 5.6 kohm, 1/4W 5% Carbon	RD1/4MB(S)562J
	R2Ø1	Resistor, 4.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)472J
	R2Ø2	Resistor, 4.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)472J
	R2Ø3	Resistor, 1ØØ ohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø1J

Parts List

9" Video Monitor 879Ø612, Model 4P Computer

Item	Sym	Description	Part Number
	R2Ø4	Resistor, 56 kohm, 1/4W 5% Carbon	RD1/4MB(S)563J
	R2Ø5	Resistor, 6.8 ohm, 1/4W 5% Carbon	RD1/4MB(S)6R8J
	R2Ø6	Resistor, 1.2 ohm, 1/2W 5% Carbon	RD1/2MB(S)1R2J
	R2Ø7	Resistor, 4.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)472J
	R2Ø8	Resistor, 22Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)224J
	R2Ø9	Resistor, 33Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)331J
	R21Ø	Resistor, 8.2 ohm, 1/4W 5% Carbon	RD1/4MB(S)8R2J
	R211	Resistor, 1Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø3J
	R212	Resistor, 68 kohm, 1/4W 5% Carbon	RD1/4MB(S)683J
	R213	Resistor, 1 ohm, 1/2W 5% Carbon	RD1/2MB(S)1RØJ
	R3Ø1	Resistor, 1Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø3J
	R3Ø2	Resistor, 1.2 kohm, 1/4W 5% Carbon	RD1/4MB(S)122J
	R3Ø3	Resistor, 2.2 kohm, 1/4W 5% Carbon	RD1/4MB(S)222J
	R3Ø4	Resistor, 1Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø3J
	R3Ø5	Resistor, 3.3 kohm, 1/4W 5% Carbon	RD1/4MB(S)332J
	R3Ø6	Resistor, 22 kohm, 1/4W 5% Carbon	RD1/4MB(S)223J
	R3Ø7	Resistor, 15 kohm, 1/4W 5% Carbon	RD1/4MB(S)153J
	R3Ø8	Resistor, 1ØØ ohm, 2W 5% Met Oxide	RSM2P1Ø1J
	R3Ø9	Resistor, 2.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)272J
	R313	Resistor, 56 ohm, 2W 5% Met Oxide	RSM2P56ØJ
	R314	Resistor, 82 kohm, 1/2W 5% Carbon	RD1/2MB(S)823J
	R315	Resistor, 15Ø kohm, 1/2W 5% Carbon	RD1/2MB(S)154J
	R316	Resistor, 22Ø kohm, 1/2W 5% Carbon	RD1/2MB(S)224J
	R317	Resistor, 1 Mohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø5J
	R318	Resistor, 22Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)224J
	R319	Resistor, 22Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)224J
	R32Ø	Resistor, 27Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)274J
	R321	Resistor, 15Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)151J
	R322	Resistor, 15Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)151J
	R5Ø1	Resistor, 1ØØ kohm, 1/2W 1Ø% Solid	RC1/2GF1Ø4K
	R5Ø2	Resistor, 47Ø ohm, 1/2W 1Ø% Solid	RC1/2GF471K
	R5Ø3	Resistor, 47Ø ohm, 1/2W 1Ø% Solid	RC1/2GF471K
	R5Ø4	Resistor, 56 kohm, 1/2W 1Ø% Solid	RC1/2GF563K
	R5Ø5	Resistor, 56 kohm, 1/2W 1Ø% Solid	RC1/2GF563K
	T3Ø1	Transformer, 15.75 KHz Drive	1Ø851ØØ1MA
	T3Ø2	Transformer, 15.75 KHz Flyback	1Ø8Ø1ØØ3YA
	TR1Ø1	IC, 2SA733(P), PNP Signal Amp	2SA733(P)
	TR1Ø2	IC, 2SC1313(G), NPN, Signal Amp	2SC1313(G)
	TR1Ø3	IC, 2SC2228Y(E), NPN	2SC2228Y(E)
	TR3Ø1	IC, 2SC536(F), NPN, Signal Amp	2SC536(F)
	TR3Ø2	IC, 2SC2373(K,L), NPN, Hor Output	2SC2373(K,L)

Parts List

9" Video Monitor 879Ø612, Model 4P Computer

Item	Sym	Description	Part Number
	VR2Ø1	Var Resistor, 1ØØ kohm	17511Ø139A
	VR2Ø2	Var Resistor, 2Ø kohm	17511Ø1ØØA
	VR2Ø3	Var Resistor, 1ØØ kohm	17511Ø139A
	VR3Ø1	Var Resistor, 1 kohm	17511ØØ5ØA
	VR3Ø2	Var Resistor, 5ØØ kohm	17511Ø16ØA
	VR3Ø3	Var Resistor, 2 Mohm	17691Ø93ØA
	VT5Ø1	Cathode Ray Tube	559Ø1ØØ4ØA

Parts List

9" Video Monitor 879Ø613 (Green Screen), Model 4P Computer

Item	Sym	Description	Part Number
	1	PCB Assembly, CRT	U31ØØ5
	1	Clip, Fuse	1973Ø3Ø8ØA
	1	Connector, Pin	19411Ø78ØA
	1	Fuse, 2A 25ØV	251ØØØ79ØA
	1	Spring, Tension	434Ø1Ø12ØA
	1	Socket, Pin	194Ø1Ø37ØA
	1	Socket, Cylindrical	19631ØØ1ØA
	1	Cord, Terminal	316Ø1Ø15ØB
	1	Cord, Terminal	316Ø1Ø14ØA
	C1Ø1	Capacitor, 4.7 uF, 5ØV Elec 2Ø%	CEØ4(RB)475M5ØV
	C1Ø2	Capacitor, 12Ø pF, 5ØV Cer 1Ø%	CK45B1H121K
	C1Ø3	Capacitor, Ø.1 uF, 5ØV Mylar 1Ø%	CQ92M1H1Ø4K
	C1Ø4	Capacitor, 22 uF, 1ØØV Elec 2Ø%	CEØ4C226M1ØØV
	C1Ø5	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C2Ø1	Capacitor, Ø.Ø22 uF, 5ØV Mylar 1Ø%	CQ92M1H223K
	C2Ø2	Capacitor, Ø.Ø22 uF, 5ØV Mylar 1Ø%	CQ92M1H223K
	C2Ø3	Capacitor, Ø.Ø1 uF, 5ØV Mylar 1Ø%	CQ92M1H1Ø3K
	C2Ø4	Capacitor, Ø.33 uF, 16V Tant 1Ø%	CS15E1C334K
	C2Ø5	Capacitor, 4.7 uF, 16V Tant 1Ø%	CS15E1C475K
	C2Ø6	Capacitor, 4.7 uF, 16V Tant 1Ø%	CS15E1C475K
	C2Ø7	Capacitor, 33 uF, 16V Elec 2Ø%	CEØ4C336M16V
	C2Ø8	Capacitor, 33 uF, 16V Elec 2Ø%	CEØ4C336M16V
	C2Ø9	Capacitor, 33Ø uF, 35V Elec 2Ø%	CEØ4C337M35V
	C21Ø	Capacitor, Ø.Ø33 uF, 5ØV Mylar 1Ø%	CQ92M1H333K
	C211	Capacitor, 22Ø uF, 16V Elec 2Ø%	CEØ4C227M16V
	C212	Capacitor, 4.7 uF, 5ØV Elec 2Ø%	CEØ4C475M5ØV
	C3Ø1	Capacitor, 22Ø pF, 5ØV Cer 1Ø%	CK45B1H221K
	C3Ø2	Capacitor, Ø.47 uF, 5ØV Elec 1Ø%	CEØ4(RB)474K5ØV
	C3Ø3	Capacitor, 1ØØ pF, 5ØV Cer 1Ø%	CK45B1H1Ø1K
	C3Ø4	Capacitor, Ø.Ø22 uF, 5ØV Mylar 1Ø%	CQ92M1H223K
	C3Ø5	Capacitor, Ø.Ø18 uF, 5ØV Mylar 1Ø%	CQ92M1H183K
	C3Ø6	Capacitor, Ø.Ø18 uF, 5ØV Mylar 1Ø%	CQ92M1H183K
	C3Ø7	Capacitor, 4.7 uF, 5ØV Elec 2Ø%	CEØ4C475M5ØV
	C3Ø8	Capacitor, Ø.Ø1 uF, 5ØV Mylar 1Ø%	CQ92M1H1Ø3K
	C3Ø9	Capacitor, 22Ø uF, 16V Elec 2Ø%	CEØ4C227M16V
	C31Ø	Capacitor, 1ØØ pF, 5ØV Cer NPO	CC45CH1H1Ø1J
	C311	Capacitor, Ø.ØØ47 uF,5ØV Poly 5%	CQ92P1H472J
	C313	Capacitor, 1ØØØ uF, 25V Elec 2Ø%	CEØ4C1Ø8M25V
	C314	Capacitor, Ø.Ø33 uF, 4ØØV Poly 5%	CQ92P2G333J
	C315	Capacitor, Ø.Ø47 uF, 4ØØV Poly 1Ø%	CQ92P2G473K
	C316	Capacitor, 1 uF, 25ØV Elec 2Ø%	CEØ4C1Ø5M25ØV
	C317	Capacitor, Ø.Ø1 uF, 63ØV Poly 1Ø%	CQ92P2J1Ø3K

Parts List

9" Video Monitor 879Ø613 (Green Screen), Model 4P Computer

Item	Sym	Description	Part Number
	C318	Capacitor, Ø.Ø1 uF, 63ØV Poly 1Ø%	CQ92P2J1Ø3K
	C319	Capacitor, Ø.ØØ47 uF, 1ØØØV Cer	CK45E3A472P
	C32Ø	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C321	Capacitor, Ø.ØØ22 uF, 1ØØØV Cer	CK45E3A222P
	C322	Capacitor, 1Ø uF, 25V Elec 2Ø%	CEØ4(RP)1Ø6M25V
	C323	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C324	Capacitor, Ø.ØØ22 uF, 5ØØV Cer	CK45E2H222P
	C35Ø	Capacitor, Ø.ØØ82 uF, 4ØØV Poly 5%	CQ92P2G822J
	C4Ø1	Capacitor, 22Ø uF, 16V Elec 2Ø%	CEØ4C227M16V
	C5Ø1	Capacitor, Ø.ØØ1 uF, 1ØØØV Cer	CK45E3A1Ø2P
	D1Ø1	Diode, 1ØE-1, Silicon	1ØE-1
	D2Ø1	Diode, 1ØE-1, Silicon	1ØE-1
	D2Ø2	Diode, VD122l, Varistor	VD122l
	D2Ø3	Diode, VD122l, Varistor	VD122l
	D3Ø2	Diode, BBT4, Silicon	BBT4
	D3Ø3	Diode, BBT4, Silicon	BBT4
	D3Ø4	Diode, BBT4, Silicon	BBT4
	D3Ø5	Diode, BBT1Ø, Silicon	BBT1Ø
	D3Ø6	Diode, BBT4, Silicon	BBT4
	DY5Ø1	Deflection Yoke	58151ØØ3ØA
	IC2Ø1	IC, AN5763, Linear V-Processor	AN5763
	IC3Ø1	IC, AN5763, Linear H-Processor	AN5763
	L3Ø1	Coil, 1Ø uH, Linearity	14341ØØ4ØA
	L3Ø2	Coil, 3Ø uH, Width	14331Ø14ØA
	R1Ø1	Not Used	
	R1Ø2	Resistor, 15 kohm, 1/4W 5% Carbon	RD1/4MB(S)153J
	R1Ø3	Resistor, 1 Mohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø5J
	R1Ø4	Resistor, 22Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)221J
	R1Ø5	Resistor, 33 ohm, 1/4W 5% Carbon	RD1/4MB(S)33ØJ
	R1Ø6	Resistor, 91 ohm, 1/4W 5% Carbon	
	R1Ø7	Resistor, 47 kohm, 1/4W 5% Carbon	RD1/4MB(S)473J
	R1Ø8	Resistor, 1 kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø2J
	R1Ø9	Resistor, 1 kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø2J
	R11Ø	Resistor, 1.5 kohm, 3W 5% Met Oxide	RSM3P152J
	R111	Resistor, 5.6 kohm, 1/4W 5% Carbon	RD1/4MB(S)562J
	R2Ø1	Resistor, 4.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)472J
	R2Ø2	Resistor, 4.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)472J
	R2Ø3	Resistor, 1ØØ ohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø1J

Parts List

9" Video Monitor 879Ø613 (Green Screen), Model 4P Computer

Item	Sym	Description	Part Number
	R2Ø4	Resistor, 56 kohm, 1/4W 5% Carbon	RD1/4MB(S)563J
	R2Ø5	Resistor, 6.8 ohm, 1/4W 5% Carbon	RD1/4MB(S)6R8J
	R2Ø6	Resistor, 1.2 ohm, 1/2W 5% Carbon	RD1/2MB(S)1R2J
	R2Ø7	Resistor, 4.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)472J
	R2Ø8	Resistor, 22Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)224J
	R2Ø9	Resistor, 33Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)331J
	R21Ø	Resistor, 8.2 ohm, 1/4W 5% Carbon	RD1/4MB(S)8R2J
	R211	Resistor, 1Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø3J
	R212	Resistor, 68 kohm, 1/4W 5% Carbon	RD1/4MB(S)683J
	R213	Resistor, 1 ohm, 1/2W 5% Carbon	RD1/2MB(S)1RØJ
	R3Ø1	Resistor, 1Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø3J
	R3Ø2	Resistor, 1.2 kohm, 1/4W 5% Carbon	RD1/4MB(S)122J
	R3Ø3	Resistor, 2.2 kohm, 1/4W 5% Carbon	RD1/4MB(S)222J
	R3Ø4	Resistor, 1Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø3J
	R3Ø5	Resistor, 3.3 kohm, 1/4W 5% Carbon	RD1/4MB(S)332J
	R3Ø6	Resistor, 22 kohm, 1/4W 5% Carbon	RD1/4MB(S)223J
	R3Ø7	Resistor, 15 kohm, 1/4W 5% Carbon	RD1/4MB(S)153J
	R3Ø8	Resistor, 1ØØ ohm, 2W 5% Met Oxide	RSM2P1Ø1J
	R3Ø9	Resistor, 2.7 kohm, 1/4W 5% Carbon	RD1/4MB(S)272J
	R313	Resistor, 56 ohm, 2W 5% Met Oxide	RSM2P56ØJ
	R314	Resistor, 82 kohm, 1/2W 5% Carbon	RD1/2MB(S)823J
	R315	Resistor, 15Ø kohm, 1/2W 5% Carbon	RD1/2MB(S)154J
	R316	Resistor, 22Ø kohm, 1/2W 5% Carbon	RD1/2MB(S)224J
	R317	Resistor, 1 Mohm, 1/4W 5% Carbon	RD1/4MB(S)1Ø5J
	R318	Resistor, 22Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)224J
	R319	Resistor, 22Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)224J
	R32Ø	Resistor, 15Ø kohm, 1/4W 5% Carbon	RD1/4MB(S)154J
	R321	Resistor, 15Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)151J
	R322	Resistor, 15Ø ohm, 1/4W 5% Carbon	RD1/4MB(S)151J
	R35Ø	Resistor, 1 ohm, 2W 5% Metal Oxide	RSN2P1RØJ
	R5Ø1	Resistor, 1ØØ kohm, 1/2W 1Ø% Solid	RC1/2GF1Ø4K
	R5Ø2	Resistor, 47Ø ohm, 1/2W 1Ø% Solid	RC1/2GF471K
	R5Ø3	Resistor, 47Ø ohm, 1/2W 1Ø% Solid	RC1/2GF471K
	R5Ø4	Resistor, 56 kohm, 1/2W 1Ø% Solid	RC1/2GF563K
	R5Ø5	Resistor, 56 kohm, 1/2W 1Ø% Solid	RC1/2GF563K
	T3Ø1	Transformer, 15.75 KHz Drive	1Ø851ØØ1MA
	T3Ø2	Transformer, 15.75 KHz Flyback	1Ø8Ø1ØØ3YA
	TR1Ø1	IC, 2SA733(P), PNP Signal Amp	2SA733(P)
	TR1Ø2	IC, 2SC1313(G), NPN, Signal Amp	2SC1313(G)
	TR1Ø3	IC, 2SC2228Y(E), NPN	2SC2228Y(E)
	TR3Ø1	IC, 2SC536(F), NPN, Signal Amp	2SC536(F)
	TR3Ø2	IC, 2SC2373(K,L), NPN, Hor Output	2SC2373(K,L)

Parts List

9" Video Monitor 879Ø613 (Green Screen), Model 4P Computer

Item	Sym	Description	Part Number
	VR2Ø1	Var Resistor, 1ØØ kohm	175llØ139A
	VR2Ø2	Var Resistor, 2Ø kohm	175llØ1ØØA
	VR2Ø3	Var Resistor, 1ØØ kohm	175llØ139A
	VR3Ø1	Var Resistor, 1 kohm	175llØØ5ØA
	VR3Ø2	Var Resistor, 5ØØ kohm	175llØ16ØA
	VR3Ø3	Var Resistor, 2 Mohm	1769lØ93ØA
	VT5Ø1	Cathode Ray Tube	559Ø1ØØ7ØA

5.6 OPTIONS

5.6.1 Graphics Board

Introduction and Programming Information

The Model 4 graphics board provides a low cost method of adding an advanced graphics function to your Model 4 CPU. The graphics board is software compatible with the Model J graphics board, but is also capable of several advanced features not found on the Model 3 board.

The Model 4 graphics board provides 640 x 240 or 512 x 192 dot graphics. The 640 x 240 dot graphics may be displayed as an independent display similar to the Model J, or it may be mixed with the 80 x 24 text display. The 512 x 192 dot graphics is always mixed with the 64 x 16 display.

The Model 4 graphics board uses a 32K byte memory. However, the graphics display uses a maximum of 19K on screen. The remaining memory is not normally visible on screen. This 32K byte memory is organized as an X - Y matrix of 128 x 256. To access the memory the CPU must set up the X and Y address register and then read or write to the desired location. However, the options control register allows the programmer to set the graphics board for automatic incrementing or decrementing of memory addresses. This makes it easy to use only 2 single accesses to memory for most situations.

A new feature provided by the Model 4 graphics board is the ability to scroll in a vertical or horizontal direction. Scrolling in the horizontal direction is controlled by the X offset register. This register scrolls one character (8 bits) for each increment or decrement of value. Scrolling in the vertical direction is controlled by the Y offset register. This register scrolls one line for each increment or decrement of value.

The following summarizes the features of the board in an I/O map format.

Port Addressing

Hex Address	Decimal	Function
80	128	Write the X register address (0-127)
81	129	Write the Y register address (0-255)
82	130	Read/write to the graphics memory specified by the X and Y address register
83	131	Write to the options control register
8C	140	Write to the X address offset register
8D	141	Write to the Y address offset register
8E	142	Write to the intermix control register

Options Control Register Description
Hex Address 83

Bit 0	0 = Graphics OFF	1 = Graphics ON
Bit 1	0 = Waits OFF	1 = Waits ON
Bit 2	0 = Increment x Reg.	1 = Decrement x Reg.
Bit 3	0 = Increment Y Reg.	1 = Decrement Y Reg.
Bit 4	0 = Read RAM & Clock X	1 = Read & Hold X
Bit 5	0 = Read RAM & Clock Y	1 = Read & Hold Y
Bit 6	0 = Write RAM & Clock X	1 = Write & Hold Y
Bit 7	0 = Write RAM & Clock Y	1 = Write & Hold Y

Notes:

1. Bit 1 should be set high all of the time, otherwise correct memory refresh is not guaranteed.
2. Bits 2 – 7 control the auto Increment/auto Decrement function, allowing a fast automatic updating of the RAM address.
3. This register is cleared on reset.

Intermix Control Register Description

HEX Address 8E

Bit 0	0 = Mixing of text and graphics is not possible, and the video display is forced into a 640 x 240 mode of operation. 1 = Text and graphics will be mixed, and the normal Model 4 control register will allow switching between 640 and 240 graphics and 512 x 192 graphics.
Bit 1	No connection
Bit 2	No connection
Bit 3	No connection
Bit 4	No connection
Bit 5	No connection
Bit 6	No connection
Bit 7	No connection

Graphics Theory of Operation

The Model 4 graphics board is designed to be a minimum chip solution for the addition of graphics to the Model 4 CPU board. The design is composed of three major elements, the dynamic RAM, the timing logic, and a gate array. Figure 5-65 shows a block diagram of the graphics board. The details of the gate array logic are shown in Figure 5-66.

A general overview of the operation of the graphics board is as follows:

> The timing logic provides all of the dynamic memory timing signals and high speed timing for the other logic. The large bulk of the work is provided by the gate array device. As shown in Figure 5-66 this gate array interfaces to the CU for memory read or write cycles. The gate array also uses video timing signals from the Model 4 CPU board to generate X and Y video addresses, and multiplexes the video addresses with the CPU X and Y counter addresses to drive the RAM address bus. The remaining logic on the board is the dynamic RAM and the shift register logic. The RAM is organized as 64K x 4; however, this organization is translated to 32K x 8 by the gate array. From the output at the RAM, the video data is latched for time synchronization and then turned into serial video data by the shift register.

The timing logic is composed of a PALIOL 8 and a 74LS74 dual flip-flop. This logic generates RAS*, CAS*, and MUX for the dynamic RAM. It also generates timing synchronization signals XADR7, STROBE1, and STROBE2. Figure 5-67 shows a timing diagram for these signals. The input signals are provided by the Model 4 CPU board and change, depending on the mode of operation. DCLK is 10.xxx MHz for 512 x 192 graphics. H, I, and J are the outputs from a counter clocked by DCLK. Figure 5-68 shows the equations for the PALIOL8.

Figure 5-65. Model 4 Graphics Controller Block Diagram

Figure 5-66. Block Diagram

Figure 5-67. Model 4 Graphics Timing Diagram

PALIOL8

# Inputs	# Outputs
1 DCLK	12 CAS*
2 J	13 RAS*
3 I	14 VIDRAMWR
4 H	15 DI
5 BDI	16 STRB1*
6 GEN*	17 CLK
7 IIN*	18 STRB2*
8 BCLK	19 XADR7
9 DJ	
11 --	

Equations

CAS*	=	(I* + H*BDI*DJ)*
RAS*	=	(J + /J X I)*
VIDRAMWR	=	(GEN*IIN)*
DI	=	I
STRB1*	=	(H*BDI* * DCLK*)*
CLK	=	DCLK
STRB2*	=	(H * BDI)*
XADR7	=	(I * DJ + I**J*)*

Figure 5-68

One unusual feature of the system timing is the CAS* signal. CAS* is clocked twice for each RAS* cycle. This allows eight bits of data to be read from memory during each RAS* cycle. The only change from the first CAS* clock to the second CAS* is the XADR7 signal. This signal is used as a column address to allow double access of RAM during each RAS* cycle.

The other signals provided by the timing logic are STROBE1, STROBE2, and CLK. STROBE1 latches data from the RAM. STROBE2 is the shift register shift-load signal. CLK is a delayed version of DCLK.

To minimize the amount of logic on the board, the gate array performs the bulk of the work. During a CPU read or write operation, the gate array timing logic forces the CPU to wait until horizontal or vertical sync. This prevents hashing on the screen. The graphics board does have a mode of operation with no waits; however, this mode is not recommended due to the possibility of memory loss. During a read cycle the first 4 bits of data are latched, then all 8 bits are latched and placed on the CPU data bus. During a CPU write cycle, 4 bits are written by the first CAS* and the last 4 are written by the second CAS*.

The Model 4 video logic provides the dot clock, horizontal sync, vertical sync, and display enable. Using these signals, the gate array generates X and Y video addresses. The start address for the X or Y counter may be changed from 0 by loading the appropriate offset register. This allows scrolling of the picture and display of all of the 32 K of memory.

The gate array also provides X and Y address counters for the CPU. These address counters may be loaded before each RAM access, or they may be programmed to automatically increment or decrement after each memory access. The outputs from the CPU X and Y address counters are multiplexed with the X and Y video address counter outputs to generate the dynamic memory addresses.

The remaining logic on the graphics board is composed of 4 devices. A 74LS245 is used to buffer CPU data into and out of the gate array. A 74LS367 is used to strobe RAM read data into the gate array. A 74LS134 is used to synchronize data from the RAMs. A 74LS166 transforms the parallel video data into serial video data which is mixed with the Model 4 CPU video.

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"R" GRAPHIC BOARD
PART NO. 8709397 REV.
REF. DWG. NO. 1700239
SILKSCREEN ARTWORK
QC GRAPHICS

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ZONE	LTR	REVISION DESCRIPTION	DATE	APPROVED
		RELEASED FOR PRODUCTION	7-19-83	
	A	DELETED RUN U4-6 TO U7-8, ADDED RUNS U4-9 TO U2-13, U2-12 TO U7-16	10-6-83 11/1/83	

RELEASED FOR PRODUCTION

REF: DRILL PLAN C1700239
PART NO. 8709397

DRAFT	DATE 5/19/83	TITLE SCHEMATIC – GRAPHICS MODEL 4
CHK'D	DATE 5/31/83	
DESIGN	DATE	
APPD	DATE 5/31/83	
APPD	DATE 7/11/83	

tandy

DWG NO 8000200 SIZE D
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TANDY SYSTEMS DESIGN
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TANDY SYSTEMS DESIGN
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SECTION VI

EXPLODED VIEWS/PARTS LIST

EXPLODED VIEW/PARTS LISTS

Contained in this section are exploded views and corresponding parts lists for the major assemblies of the Model 4P Portable Computer. These exploded views are divided into four major assemblies:

Case Assembly
Main Chassis Assembly
Disk Drive Assembly
Keyboard Assembly

Case Assembly

Model 4P Computer

Parts List, Case Assembly

Model 4P Computer Assembly

Item	Qty	Description	Part Number
1	1	Case Housing	8719346
2	1	Cover, Front	8719348
3	2	Clawbolt	8569190
4	2	Latch Guard	8719406
5	1	Keyboard Stop, Cover	8779186
6	1	Pocket, Inside	8719348
7	1	Handle, Case	_____
8	2	Rivet, Blind	8579049
9	1	Power Cord	8709475
10	2	Clip, Cord	_____
11	4	Screw, 8-32 x 1/2" Truss Head	8569203
12	2	Screw, #10-32 x 1/2" PPH	8569202
13	1	Label, Handle	_____
14	1	Door, Rear Panel	8719349
15	1	Retainer, Door	8729252
16	5	Fastener, Springrip	_____
17	2	Rivet, Blind	_____

Chassis Assembly

Parts List, Chassis Assembly

Model 4P Computer Assembly

Item	Qty	Description	Part Number
1	1	Chassis Weldment	8859Ø28
2	1	Connector, Power Cord	8519Ø13
3	1	Fan, 12 VDC	879Ø4Ø6
4	1	Bracket, Switch Mount	8719363
5	1	Potentiometer, 5ØØ ohm Contrast	826115Ø
6	1	Potentiometer, 5ØØ kohm Brightness	826245Ø
7	1	Power Switch, 125V	8489Ø73
8	1	Reset Switch	8489Ø71
9	1	CRT/Sweep PCB Assembly,B/W	879Ø612
		CRT/Sweep PCB Assembly, Green	879Ø613
1Ø	1	Insulator, Sweep PCB	8539Ø5Ø
11	8	Clip, Standoff	8589Ø84
12	1	Mount, Power Supply	8729246
13	1	Insulator, Power Supply	8539Ø49
14	1	Power Supply PCB Assembly	879ØØ49
15	1	Cover, Back	8729243
16	1	Support, Handle	8729242
17	1	Bezel	8719341
18	2	Clawbolt Top	856919Ø
19	2	Stiffener, Bezel Case	872928Ø
2Ø	2	Knob, Potentiometer	8719362
21	1	Logo, Model 4P	8719367
22	1	Main PCB Assembly	_____
23	1	Pan Assembly, PCB Support	8729245
24	1	Cover Plate (Blank)	8729253
25	1	Cover Plate (I/O Port)	8729287
26	1	Label, FCC Part 15 Class A	_____
27	1	Label, FCC Part 15 Class B	_____
5Ø	22	Screw, #6 x 1/4" Rolok	8569128
51	4	Screw, #8-32 x 1/2" Washer Hd	8569Ø2Ø3
52	4	Washer, #8 Internal Lock	_____
53	4	Screw, #8-32 x 3/8 PH	8569Ø2Ø5
54	6	Screw, #8 Hex Washer Head Thd Form	8569Ø2Ø3
55	2	Screw, #4-4Ø x 3/4" PH Chrome	8569221
56	2	Nut, #4-4Ø Lock	8579Ø48
57*	2	Screw, #1Ø-32 x 1/2" PPH	8569Ø2Ø2
58	8	Screw, #6-32 x 3/8" PPH	8569Ø1Ø8
59	2Ø	Screw, #6 x 1/4" Hex Hd Torque Brk	_____
6Ø	2	Screw, #1Ø x 1/2" Hex Hd Thd Form	_____
61	2	Screw, #4-4Ø x 1/4 PPH Mach	_____

*Noted on Case Assembly also

Disk Drive Assembly

Parts List, Disk Drive Assembly

Model 4P Computer Assembly

Item	Qty	Description	Part Number
1	1	Weldment, Support	8859Ø29
2	2	Disk Drive, Tandon TM 5Ø-1	879Ø121
3	1	Cable Assembly, FDC	87Ø945_
4	1	Cable Assembly, DC Harness	87Ø9456
5	2	Handle, Disk Drive	8719353
6	7	Screw, 6 x 1/4" Rolok	8569128
7	6	Screw, 6-32 x 1/4" PPH Mach CSRS	_____

Keyboard Assembly

Model 4P Microcomputer

Parts List, Keyboard Assembly

Model 4P Computer Assembly

Item	Qty	Description	Part Number
1	1	Bottom, Keyboard Case	8719342
2	1	Keyboard Assembly	879Ø53Ø
3	1	Top, Keyboard Case	8719343
4	1	Cable Assembly, Keyboard	871946Ø
5	4	Spring, Keyboard Support	8719Ø14
6	2	Support, Keyboard	8719336
7	1	Cable Tie	8559Ø27
8	1	Nameplate, Keyboard	8719367
9	8	Screw, #6 x 1/2" Thd Forming	_____